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## Abstract

With the advent of miniaturised sensors for various engineering and medical applications there is an increased demand of low-power, low-voltage analog building blocks like opamps and OTAs. Degradation of certain amplifier characteristics with supply voltage is a major concern for low-voltage design and often poses contradictory requirement. CMRR (common mode rejection ratio), one such feature, is essential for sensing small bio-electric signals riding over large common-mode voltage. Here we focus on the challenging task of building a low-voltage OTA with high CMRR along with wide CMR (common mode range) and high output impedance. Robust tail current sources for a complementary differential pair OTA with folded cascode output is implemented for the purpose. The circuits are designed and simulated in 0.35 mum standard CMOS technology with supply voltage of 1.8 V. We could demonstrate a maximum of upto 40 dB increase in CMRR for a range of common-mode voltages.

# Low-voltage high CMRR OTA for electrophysiological measurements

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***Abstract*— With the advent of miniaturised sensors for various engineering and medical applications there is an increased demand of low-power, low-voltage analog building blocks like opamps and OTAs. Degradation of certain amplifier characteristics with supply voltage is a major concern for low-voltage design and often poses contradictory requirement. CMRR (common mode rejection ratio), one such feature, is essential for sensing small bio-electric signals riding over large common-mode voltage. Here we focus on the challenging task of building a low-voltage OTA with high CMRR along with wide CMR (common mode range) and high output impedance. Robust tail current sources for a complementary differential pair OTA with folded cascode output is implemented for the purpose. The circuits are designed and simulated in 0.35$\mu$m standard CMOS technology with supply voltage of 1.8V. We could demonstrate a maximum of upto 40dB increase in CMRR for a range of common-mode voltages.**

## I. Introduction

Scaling of modern integrated circuit technologies as well as increasing battery- and solar-powered systems demand more and more circuits to work at very low supply voltages. However, while digital circuits can work without too many problems in such conditions, new analog architectures must be developed to maintain their performance. The problem for analog circuit design worsens as the threshold voltage reduction is not linear with that of the supply. Various performance criteria of an OTA suffer greatly due to this. Amongst these, degradation of common-mode rejection ratio (CMRR) is one of the major issues. In cases where small differential signals are to be picked up from a noisy environment with varying common mode voltage, like recordings from brain tissues for prosthetics or experimental setup, a high CMRR is essential.

Various high impedance tail-current sources are used in OTA for a better CMRR, but a low supply voltage restriction limits their usability. Reduced voltage hampers the output impedance and input common mode range (ICMR) of the OTA. This is a major concern when bio-electric signals are to be recorded from tiny micro-electrode arrays (MEA) having small power budget and working with small batteries for increased life time and portability. These OTAs are typically placed very near to the recording electrodes, are used as pre-amplifiers (with limited demand for gain) and operate on signal bandwidths less than a few kilohertz. A design trade-off has to be arrived upon considering all these issues. CMRR degradation can be attributed to a low resistance tail current source that keeps varying with common-mode voltage. An improved tail-current source was proposed [1] to overcome the problem of CMRR faced particularly at low voltages. The design constituted of a simple 5-transistor OTA (P channel input) showing a remarkable increase in CMRR. However, a 5-transistor OTA suffers from various other performance limitations when low supply voltages are concerned. Here we enhance the concept by using complementary differential input pairs for rail-to-rail input common-mode range, and a folded cascode stage to increase output impedance of an OTA.

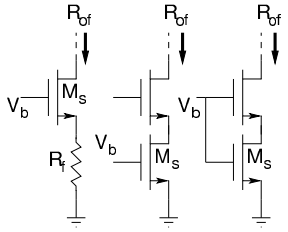


Fig. 1. Conventional methods of increasing $R_{of}$ of a current source uses stacked transistors in series increasing the compliance voltage of the source. $M_s$ is the transistor deciding the magnitude of output current $I_o$

## II. High impedance tail-current source

Theoretical study of differential amplifiers and OTAs show an inverse relationship between CMRR and the conductance of the tail current source. A more elaborate study [2] shows detailed analysis of CMRR at low voltages, with complementary differential pair, consisting of a systematic and a random component both following similar relation. The systematic CMRR is topology dependent where as the random CMRR is function of both topology and mismatch. Here we deal with the systematic CMRR which when enhanced improves random CMRR as well. Various methods of creating high impedance tail current source exists in literature but neither are very well suited for low voltage application. This is primarily because they all use some variants of series-series feedback topology stacking multiple transistors in series. This consumes at least $2V_{DS(sat)}$ or more compliance voltage for the current source. Examples like source degeneration, cascode or self cascode are some popular methods shown in Fig.1. In all cases the feedback voltage varies the source of the top transistor while

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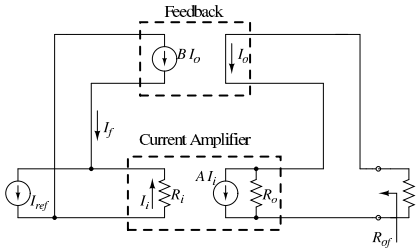


Fig. 2. Generic Shunt-Series feedback topology. $R_{of}$ is the output impedance seen by the load $R_l$. The current amplifier is shown in the inset.

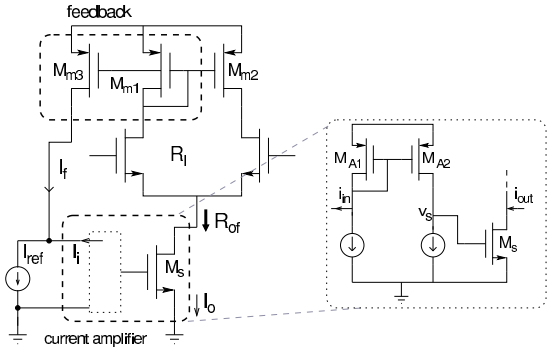


Fig. 3. Implementation of Shunt-Series feedback for the tail-current ($I_o$) of a simple differential pair (acting as load).

keeping the gate constant. The feedback loop ensures a high output impedance $R_{of}$ seen by the load ($R_l$, not shown). It can be deduced as: $R_{of} = R_f + (1+A)r_o$. Where $r_o$ denotes the actual output resistance of the top transistor, $A$ is the gain provided by the feedback loop and $R_f$ is the resistance of the object used for feedback (a resistor or a transistor). However, stacking transistors in series inherently increases the compliance voltage of the current source. Allocation of this much voltage for the tail current source seems impractical for low-voltage design. Instead, if the feedback could directly control gate voltage of the current source, a single transistor could effectively produce a high output resistance. Shunt-series feedback offers us such an opportunity. In [1] the compliance voltage is decreased by more than half and the feedback gain is greater than a cascode stage increasing the $R_{of}$ of the source even higher.

## III. Shunt-Series: theory and implementation

Theoretically shunt-series feedback has the capability to increase the output impedance in the same manner as the series-series version.

In both series-series and shunt-series topology the output variable is $I_o$, where as, the input is a voltage source ($V_b$) or current reference ($I_{ref}$), respectively (Fig.2). In the later case, as a portion of the sampled output current is fed back instead of converting it into voltage. The basic shunt-series configuration shown here consists of a current feedback and a current amplifier. The circuit in Fig.3 demonstrates how this idea can be implemented by MOS current source $M_s$. It can be immediately noticed that the parts of the feedback circuit fits easily as a current mirror of a differential amplifier. The output of the current amplifier circuit (described later) can be considered as the tail current source ($M_s$) and the differential pair themselves become the load ($R_l$) to the feedback circuit. From Fig.2 the relation between $I_o$ and the reference can be obtained:

$$I_o = A(I_{ref} - \beta I_o) = \frac{A}{1+A\beta} I_{ref} \approx \frac{I_{ref}}{\beta} \qquad (1)$$

Keeping $\beta$ =1, we can use $I_{ref}$ as the predefined tail-current of the differential pair. In Fig. 3 if the feedback transistor $M_{m1}$ is used as part of the current-mirror load of the OTA it will carry only $\frac{I_o}{2}$ (flowing through one half of the differential branch), hence we need to double the geometry of mirrored transistor $M_{m3}$ for unity feedback. From the direction of $I_i$ we can see, $I_i$ = $I_{ref}$ - $I_f$, which ensures a negative feedback.

## IV. Current Amplifier

The obvious way to amplify current is by geometry of a current mirror, but a large gain essential for the feedback loop requires huge transistors that are unacceptable. Simple high gain current-mode differential amplifiers are reported in literature [3]. Single ended version of such an amplifier (with correct polarity) can be used to produce a high enough gain for the forward path in this feedback circuit. From Fig. 3(inset) we have: $i_{out} = g_{Ms} v_s$, and $v_s = i_{in}(r_{o1}||r_{oM2})$. Hence the small signal current gain($A$) is $g_{Ms}(r_{o1}||r_{oM2})$. Here $r_{o1}$ is the resistance of the current bias.

## V. Design of the OTA

We will first incorporate the shunt-series feedback circuit into a n-channel differential amplifier with folded cascode output. The circuit in Fig.4 shows such an implementation where the differential input (center) and the cascode output (right) is easily recognizable. The left part of the circuit is responsible for the feedback loop. However, in a conventional folded cascode circuit, the bias current sources $I_B$ sits on top and the mirror circuit at the bottom part of the cascode stack. Hence the currents $i_1$, $i_2$ from the N differential pair is normally folded by P type current sources and mirrored by N type mirrors. In contrast, here the folding and mirroring both are done with P type mirrors. As shown in the diagram, this method also produces the expected small signal out currents ($i_2$-$i_1$) and is better suited for shunt-series feedback configuration. Transistor $M_{m1}$ which belongs to the current mirror stage on top right can be used as the feedback transistor as before. However, now it carries two dc current components: $\frac{I_o}{2}$ (from one of the differential pair) and $I_B$ (from the current source below). While using $M_{m1}$ in feedback loop, $I_B$ should be subtracted from the mirrored current in $M_{m3}$ before passing it to the CA(current amplifier). The bias currents ($I_B$) are created from cascode current sources and high swing current mirrors are used to increase the output swing of the OTA. In this circuit, we kept the feedback ratio ($\beta$) as unity by using a 1:1

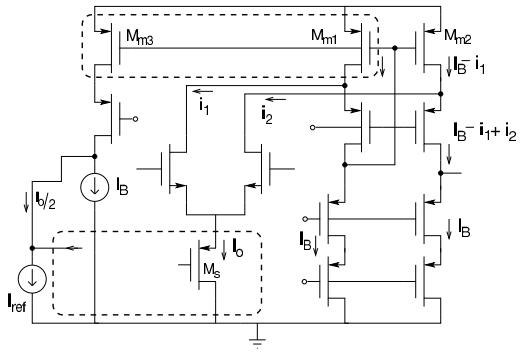


Fig. 4. A folded cascode amplifier using shunt-series mechanism. The feedback current has an additional component ($I_B$) to it. The cascode stage uses a low-voltage current mirror to reduce voltage headroom.

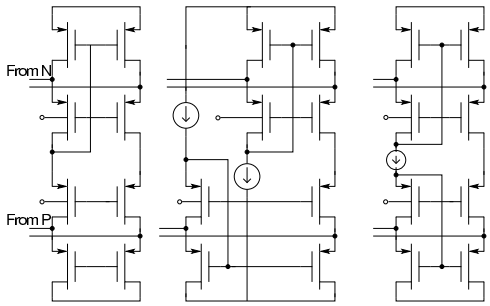


Fig. 5. Current summing output stages for complementary differential pair input. A conventional one is shown on the left, the circuit used for simulations is shown in the middle and a better implementation of the same is shown on the right.

current mirror in feedback path but setting the $I_{ref}$ as twice the value of the required tail-current source.

In conventional complementary differential pair as input, the current signals from the differential pairs are summed up by folding one of them (say P) at the bottom of the stacked branch and mirroring the other (Fig. 5,left) from top half. In the feedback scheme we are using, current feedbacks for both P and N differential currents are essential. This can be obtained with mirrors on both half of the stacked transistors and has been reported in [4] (Fig.5,middle). Two different feedback circuits are used to regulate the two tail current sources (not shown), one for N and one for P differential pair. A further improvement on the output is to remove the separate biases for the two output current mirrors to a single floating current source biasing both of them (Fig.5,right). This has been shown to reduce offset for such current summing stages [4]. For sake of simplicity, in the next section we only show the simulation results with two separate current biases.

## VI. Simulation Results

We simulated the OTA in 0.35$\mu$m process from MOSIS with 1.8V supply using the TSPICE simulator. In the simulations we compared the proposed OTA (labeled as *C*) with a classical complementary differential pair OTA having folded cascode output but without the CMRR enhancement circuits (labeled as *A*) [6]. Another OTA (labeled as *B*) similar to *A* but having cascode tail current sources for each differential pair

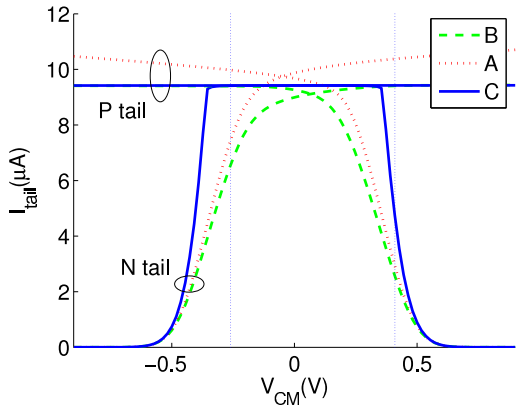


Fig. 6. Variations in tail currents while varying the common-mode voltage ($V_{CM}$) from rail to rail. Solid lines represent the tail-currents for the proposed circuit and dotted shows results from an OTA without the current-shunt mechanism. Dashed lines show the result from a similar OTA with a cascode tail current source. In between the vertical bars neither of the cascode current sources reached their saturation currents. This is a problem particular for low voltage operation.

[6] was also used for comparison. Simulation results from the three topologies are plotted in dotted (*A*), dashed (*B*) or solid (*C*) line. The results show a prominent increase in the performances related to common mode rejection. We compare our results over a wide common-mode (CM) input range. While plotting common-mode voltage ($V_{CM}$) on x-axis, we denote mid-supply (0.9V) as zero and vary $V_{CM}$ on either side of it.

In Fig. 6, the P and N tail current are plotted while the $V_{CM}$ is varied from rail to rail. Shunt-series feedback expectedly increases the impedance of the tail current than other implementations producing much flatter $I-V$ curve once the compliance voltage is reached. The saturation values of the tail-current is dependent on the gain of the current amplifiers. It can be noticed that both the cascode tail current (in *B*) reaches an impedance comparable to *C* while $V_{CM}$ approaches the opposite supply rail. This clearly reflects the increased compliance voltage of the cascode current source. Around a region on either side of the mid-supply voltage ($V_{CM} = 0$), none of the two tail current sources in *B* reached the saturation current (marked by vertical blue lines). This is a serious issue where a high CMRR is required for a wider input CM range. As supply voltage drops, this region gets wider.

Gain, UGB (unity gain bandwidth) and PM (phase margin) of the three OTAs for different CM values are shown Fig. 7. All simulations are done with a closed loop configuration where the OTA output voltage is determined by the CM input value. Hence there is a limited range of $V_{CM}$ around the midsupply for which the output transistors are in saturation. All three amplifiers, working in low 1.8V supply voltage, show a degradation in differential mode gain 300mV away from the midsupply. The gains start dropping even faster when $V_{CM}$ moves more than 500mV away from the midsupply. Results from all three topologies are comparable where gain, UGB and PM are concerned. The only dominant pole occurring

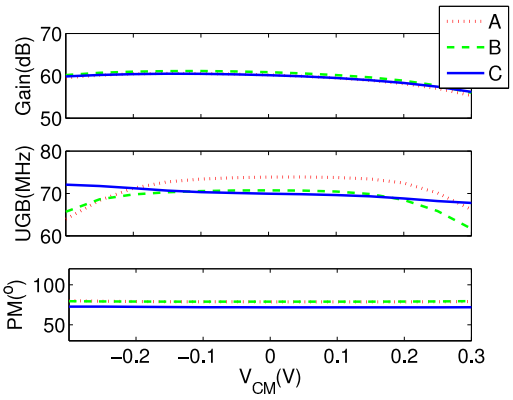


Fig. 7. All the three configuration show similar low frequency differential gains. The gain decreased withing 400mV of the mid-supply voltage because of the closed loop measurement technique. Current-mode amplifiers in feedback path of design *C* was compensated to reduce effects of additional poles and zeros in UGB and PM results. All results are plotted for a 10kHz operating frequency.

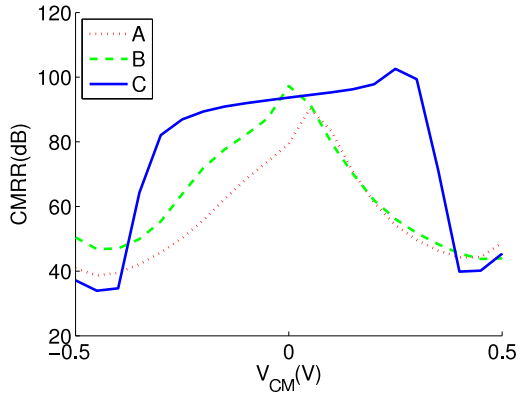


Fig. 8. Comparison of CMRR at 10kHz shows a much more stable result from the proposed scheme compared to the other two. The CMRR is also computed in a closed loop fashion (matched source method in [5]).

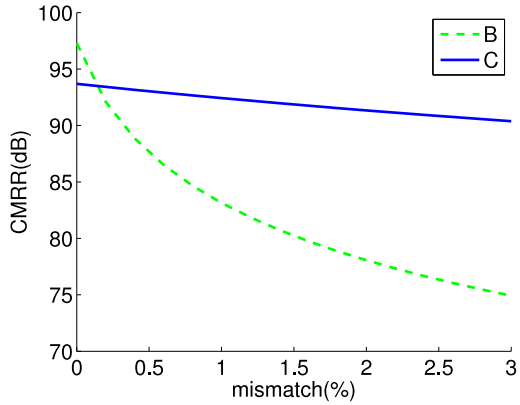


Fig. 9. One of the input transistors was varied over up to 3% in width while measuring the CMRR at 10kHz keeping the CM at 0.9V.

from the output node determines the 3dB cutoff frequency of the OTAs. The current-mode amplifiers in the proposed OTA (*C*) was compensated with 100fF capacitors pushing all its non-dominant poles and zeros at higher frequencies. The gain and the bandwidth ($\sim$ 100kHz) obtained from *C* is enough for the application proposed. For a step input in a follower configuration, the output follows the input close to within 100mV of the supply rail (not shown).

Electrophysiological signals from intracellular recordings or from LPF (local field potential) can be recorded comfortably with few kHz bandwidth. As this OTA is considered to be the pre-amplifier sitting close to the actual site of recording, $\sim$ 60dB gain is enough where a low power dissipation is essential.

Simulation of CMRR can be done in many different methods [5]. We used a simple method called *matched source* setup that uses two matched ac sources as input and produces a direct CMRR measurement at the output [6]. As shown in Fig. 8 The CM voltage is changed while measuring CMRR (at 10kHz) for all three topologies. Systematic CMRR for both *A* and *B* drops steadily on either side of mid-supply. As the differential gain remains same for the entire range, the common-mode gain (in *A* and *B* compared to *C*) is to blame for nearly 40dB drop in CMRR. Due to drop in the differential gain outside the 600mV around midsupply (as described before), the CMRR also start to drop. Fig. 9 illustrates random CMRR degradation on increasing mismatch. An input differential pair was tested by varying the width of one transistor while keeping the $V_{CM}$ constant (0 in this case). The shunt-series current source expectedly outperforms the cascode current source due to its higher output impedance over wider common-mode range.

## VII. Conclusion

We described a low-voltage OTA suitable for electrophysiological recordings that can be fabricated on tiny microelectrode arrays. The OTA uses a complementary differential pair input and folded cascode output both highly suitable for such low-voltage low-power application. The main advantage is its large CMRR ranging over wide range of common-mode voltage ($V_{CM}$).

## VIII. Acknowledgememnt

This work was supported by the Swiss National Science Foundation grants PP00A106556 and PBEZ2-121231, and ETH grant TH02017404.

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