FULLY PROGRAMMABLE BIAS CURRENT GENERATOR WITH 24 BIT RESOLUTION PER BIAS

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ABSTRACT

This paper describes an on-chip programmable bias current generator, intended for mixed signal chips requiring a wide ranging set of currents. The individual generators share a master current reference. A serial digital interface to the chip controls the biases by bits loaded into a 24-bit shift register. These bits control the steering of current from a current splitter. The summed current splitter output is actively mirrored to a broadcasted bias voltage. Measurements from an implementation in 0.35u 4M-2P CMOS show a total range of bias current of over 6 decades (>120dB) ranging from a few times the off-current up to the master reference current. For currents larger than the minimum, the generator has resolution spanning nearly its full 24 bit range (144dB), e.g. for a master current of 10uA, any bias current can be varied by as little as 0.5 pA with the caveat that the code is not guaranteed monotonic. Each bias occupies an area of 0.026 mm^2, which is about 65% of the bonding pad that it replaces. Measured variation in generated currents is <10% in strong inversion and about 20-30% in weak inversion.

1. INTRODUCTION

We earlier reported a design kit for generating wide ranging fixed bias currents [1, 2]. These circuits compact and are suitable for chips with known biasing requirements for very wide ranging currents, when the fixed currents need only be resolved to within the nearest factor of two. However it is often the case with complex chips that the required currents are not known ahead of time or that they need to be changed during operation. In general it is desirable to avoid any off-chip analog components, especially if they require high precision. Using off-chip voltage DACs that drive gate voltages is an interim solution to programmability. It is a very poor solution if one considers the cost in pin count, temperature and process sensitivity, board complexity, and cost. Here we report a completely programmable integrated bias current generator with a simple digital interface.

2. IMPLEMENTATION

The system level diagram is shown in Fig. 1. A microcontroller (uC) interfaces between the chip and a controller PC. The SPI (Serial Peripheral Interconnect) interface to the bias generator uses 3-8 wires, depending on desired functionality and testability. At a minimum, Clock, IN, and Latch input are required. We also use the master bias power-down input Power-down to turn off all currents and we generally use an off-chip resistor R_{master} instead of the integrated resistor, bringing the total to 5 pads. Other pads provide access to the master bias voltage gate voltage and to n- and p-type test transistor gate and drain terminals. Shift register output OUT can be tied to the next chip in series, if desired.

As before [1, 2], we assume that the design requires a fixed transconductance, rather than a fixed current or precise reference voltage.

All biases are controlled by a single Sivilotti-type [3] single-phase register (SR); each bias uses 24 bits of the shift register to steer the current in a 24-bit octave current splitter [1, 2, 4]. The input to each current splitter is a copy of the master bias current I_m. Thus each bias can in principle be any fraction of up to 24 bit resolution of the master current. Level-sensitive latches (L) are made opaque (Latch high) while new bias settings are loaded and then transparent to transfer the SR outputs to the current multiplexer switches. The output from the splitter is steered to a dual n- and p-type 'current buffer' (CB) consisting of two active mirrors, which serve to isolate the splitter from the rest of the chip and to greatly lower the bias voltage impedance [1, 5]. The buffers are biased with the master current. The outputs of the buffers are the n-bias and p-bias voltages that are used in the chip core.

These circuits were fabricated in the AMS 0.35u 4M-2P process as part of a vision sensor chip with 12 biases. Fig. 2 shows a micrograph of the entire generator and layout of a single splitter cell. Common centroid layout was not used but may improve splitter ratio matching. Dummy splitter cells at the ends were used, and metal coverage of the splitter transistors was made as identical as possible. A complete 12-bias layout in 0.35u occupies an area of 0.63 mm^2, or about 13% of a minimum sized Europractice or MOSIS design. Each individual bias has an area of 0.026 mm^2—about 65% of the bonding pad it could replace.

A Windows XP software infrastructure was built to interface transparently to either a Cypress FX2 USB2

microcontroller using the Thesycon Java USB driver or to the Silicon Labs C8051F320 USB1 controller using the Silicon Labs USBXPress driver. The biases can be controlled using the Java classes directly (e.g. from matlab) or through a Java GUI. Persistence is implemented in software at present, but it is planned that the biases will be stored in flash memory on the chip's associated microcontroller. The 8051 controller receives USB control transfers from a PC and forwards them over the SPI interface to the chip. A Keithley 2340 SMU was used to measure the currents produced by the generated bias voltages using test transistors placed inside the master bias block.

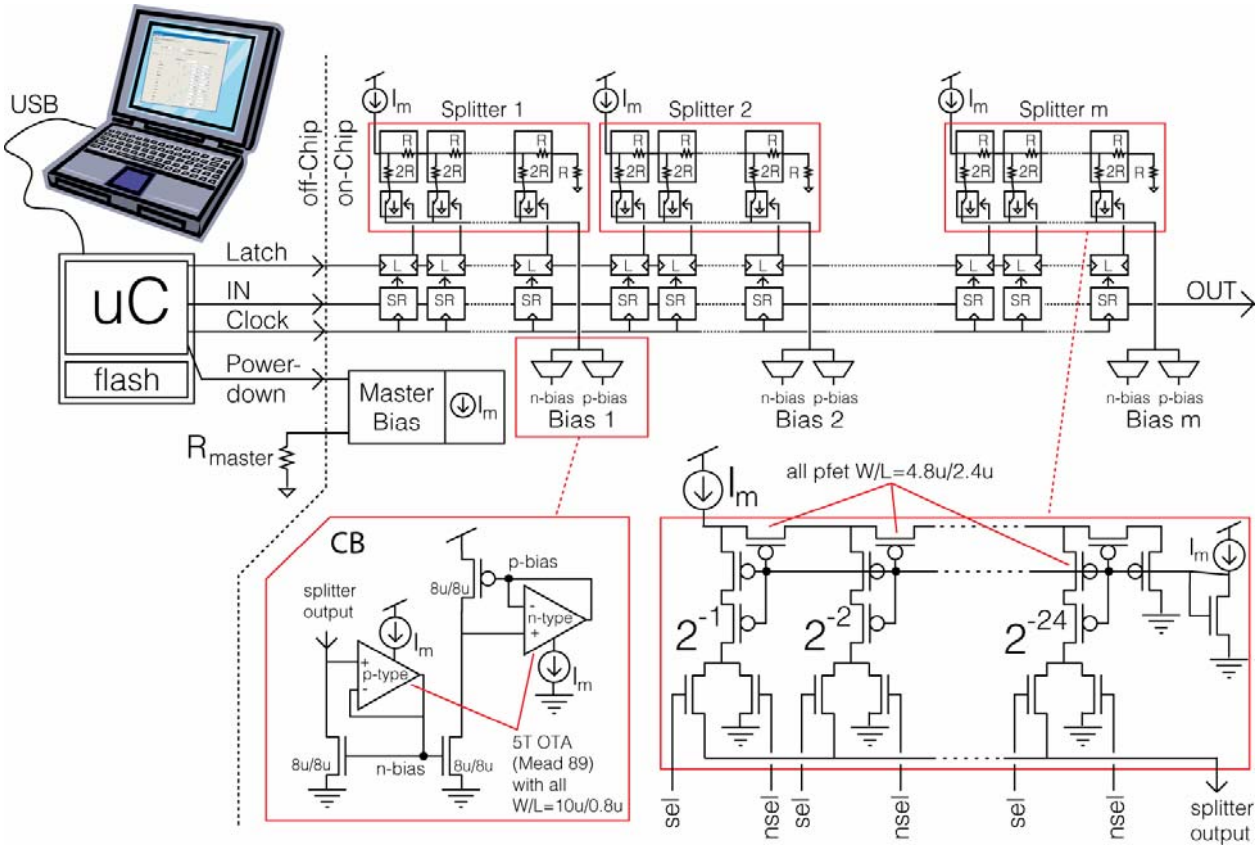

Fig. 1 Bias generator system-level architecture.

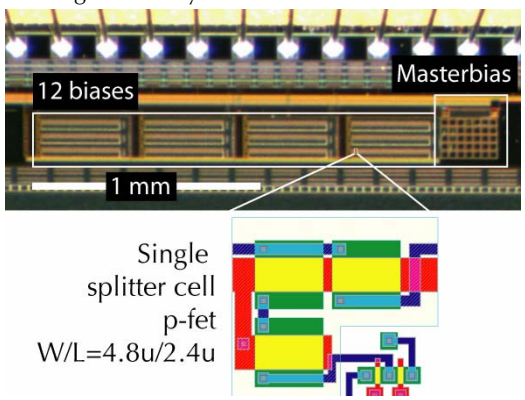

Fig. 2 Micrograph of fabricated circuit and drawn layout of a single splitter cell.

3. CHARACTERIZATION RESULTS

The measured characteristics in Fig. 3 show that each bias can be adjusted over a range from I_m down to a few times the transistor off-current I_0—in the case shown, from a few uA down to a few pA. This overall dynamic range of 120dB, (6 decades, or 20 bits), is limited by the off-current that sets a minimum current that can be copied by a standard current mirror [5]. Fig. 4 shows that the actual resolution of the current extends down several more bits, so the effective resolution of the bias current is nearly 24 bits as long as the current is at least a few times the off-current and some non-monotonicity can be tolerated.

Detailed analysis of statistical variation is beyond the scope of this short report. However, Fig. 5 shows another view of the data in Fig. 3. Each tap's current is multiplied by the ideal octave factor. N- and p-type biases differ only in the additional active mirror in CB, so presumably the difference between n-type and p-type arises from an Early effect. Mismatch is about 20-30% CV in the subthreshold region of operation and <10% in strong inversion. This variation is insignificant for prototyping (where it is

already vastly improved compared with gate voltage biasing) but it could be significant for large-scale production and testing if biases require individual calibration. Although individual bits are guaranteed by the splitter operation to be monotonic, non-monotonic sub-tap behavior could be significant when biases are changed dynamically in an active feedback loop. Fig. 6 plots for all 10 biases on one chip the ratios between the currents $I(2^k-1)$ and $I(2^k)$, e.g. between DAC values 0111 1111 and 1000 0000. This ratio should be less than one for monotonicity and this is the case 74 % of the time.

The dynamic response of a bias to a change in level is shown in Fig. 7. After a new value is loaded, the bias voltage settles to the new level within a few us, much faster than the ~1 ms required for loading new values over the SPI interface. During loading, the bias is perturbed by a few tens of mV by the bias clock, but at least for our applications this coupling will not be a substantial drawback. In any case it may arise at least in part from the prototype arrangement.

Fig. 8 shows how a generated bias voltage responds to a disturbance. A bias was perturbed by a 200mV step applied to a 150 pF capacitor tied to the bias. The curves show the bias voltage step-disturbance response for different measured bias currents. Because the bias is actively buffered by CB, the response to disturbance recovers in <10 us and is only a weak function of bias current; over 5.5 decades of bias current the recovery time changes by about a factor of 10. As predicted in [1], there is a slight resonance at an intermediate bias current.

The circuit layout intentionally used a p-type current splitter (as in [1] but different than e.g. [5]) despite the observation that p-fet matching is generally worse than n-fet matching [6], sometimes as much as 10x worse [7]. Matching was optimized by using large unit transistors and ensuring equivalent metal coverage; metal1 did not cross any channels (Fig. 2). P-fets were used because on vision sensors they can be protected from parasitic photocurrent effects [1]. This capability is demonstrated in Fig. 9. Compared with [1], the already-small influence of light has been reduced from a 20-40% effect to nearly immeasurable—how much exactly is hard to say because we could not measure any change in current except at the currents very near the off-current, even under irradiance of 30 W/m^2 by deeply-penetrating long wavelength incandescent illumination. The slight decrease in the smallest significant currents is consistent with additional photo-induced junction leakage from splitter p-fet source/drains to Vdd. This improvement was achieved by more carefully shielding every part of the bias generator with metal, including the master bias and the ends of the current splitters, and by surrounding all n-fets with uninterrupted n-well guard bars (tied to a supply rail, generally Vdd) that are at least 5 um wide.

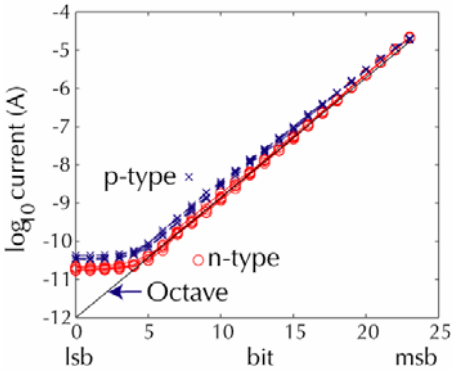

Fig. 3 The measured current from 10 biases on the chip (5 are n-type, 5 are p-type) as a function of the splitter tap. Line shows ideal octave behavior. Measured I_{0n}=0.3 pA.

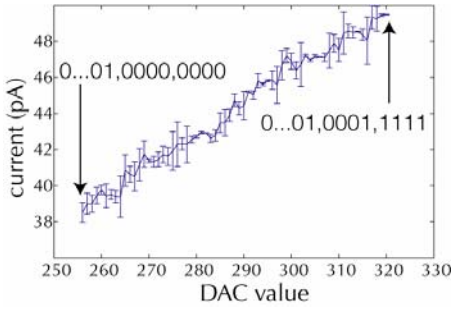

Fig. 4 Shows the effect of the lowest 6 bits of the 24 total per bias, with bit 8 turned on. Error bars show measurement variation with n=21.

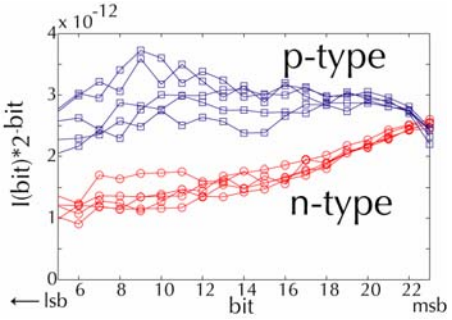

Fig. 5 The currents of Fig. 3 scaled by the ideal octave multiplier.

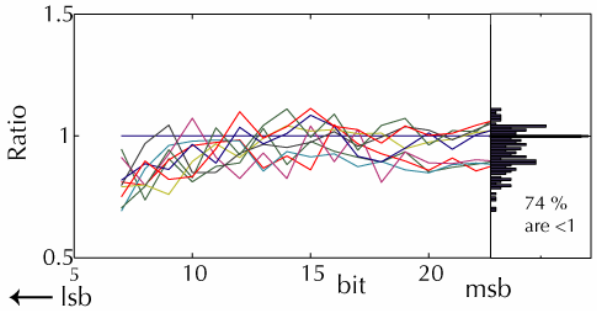

Fig. 6 Measurement of monotonicity, showing for 10 biases the ratios $I(2^k-1)/I(2^k)$.

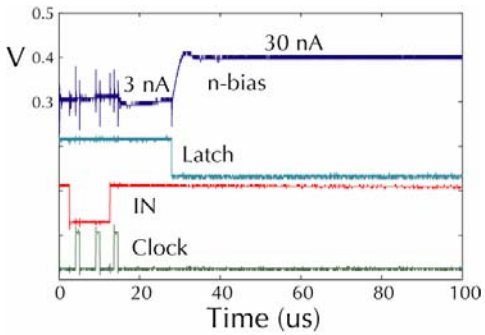

Fig. 7 Shows the dynamic response of a bias voltage to a 10x change of bias current.

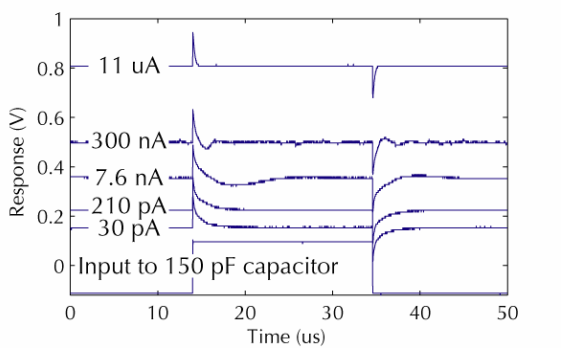

Fig. 8 Response of a generated bias to external disturbance. Measured I_m=27uA.

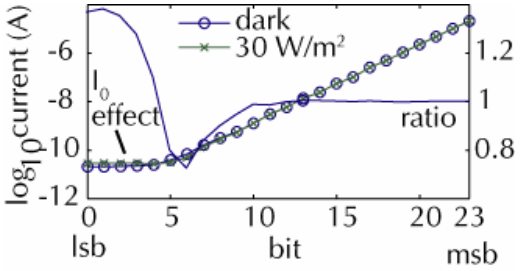

Fig. 9 Effect of light on a generated bias current.

The supply current for the generator consists of $2I_m$ for the master bias plus $3I_m$ for each bias; for the instance reported here with 12 biases and with I_m=27 uA, the total biasing supply current is ~300 uA, or 1% of the chip supply current of 30 mA.

4. DISCUSSION

We described an on-chip programmable bias generator circuit. The chip interface is a standard SPI serial interface. The fabricated circuit has 6 decades of overall range, but altogether a (possibly non-monotonic) resolution of better than 10^{-7} of the master current. The currents that are produced have PTAT-like characteristics, resulting in relatively constant-g_m behavior (with the caveats clearly pointed out in [8]). 12 biases can be loaded over SPI in <1 ms, and they settle to new values in a few us.

After 3 months satisfactory application-level experience [9], the major limitation discovered is in the current buffers, which should be redesigned to avoid excessive overdrive that limits their output swing too far away from the rails, thus preventing simultaneous large I_m and tiny bias current.

These circuits will especially advance application of neuromorphic analog VLSI—which often relies on a wide range of biases—in real-world scenarios, where it is awkward and bulky to use passive potentiometers or off-chip DACs and where temperature and process insensitivity matters a great deal. Most important, it will allow feedback control of these chip-level parameters. To aid developments by other designers, we will place Tanner tools schematics and layout of the fabricated AMS 0.35u circuits on our web site at http://www.ini.unizh.ch/~tobi/biasgen.

5. ACKNOWLEDGEMENTS

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6. REFERENCES

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