Design of Amplifier with Rail-to-Rail CMR with 1V Power Supply

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Abstract

The continuous reduction of power supply voltage for VLSI circuits put forward new challenges for analog designers. In this paper we present a low-voltage CMOS amplifier with rail-to-rail input common-mode range. The amplifier was designed with 1V supply voltage in standard digital technology. Alternative methods were applied for obtaining high ICMR, good CMRR and output swing at such low supply voltage. A bandgap reference was designed with same supply using current-mode technique.

1. Introduction

Scaling of modern integrated circuit technologies as well as increasing battery- and solar-powered systems demand more and more circuits to work at very low supply voltages. However, while digital circuits can work without too many problems in such conditions, new analog architectures must be developed to keep similar performance with respect to operation at higher supply voltages. The problem for analog circuit design gets exaggerated because; threshold voltage reduction is not linear with that of the supply. For low supply voltage, amplifiers suffer greatly from reduction in ICMR. Complementary differential pairs with g_m stabilization circuits are used to extend the input common-mode range towards both the supply. This requires a minimum of $4V_{ds,sat} + 2V_t$ of supply which is around 1.4V in standard digital process [1]. Hence, it is not recommended for a 1V technology. This paper discusses methods to overcome this and some other related problems like degradation of CMRR, in a low-voltage amplifier. It also uses a reference generator of bandgap type but with 1V supply. Unlike the conventional bandgap reference that generates 1.2V and requires a minimum of 1.5V supply voltage, current-mode technique was used. It will be shown that this can reduce the power supply constraints considerably. The circuits were implemented in 0.35µ standard CMOS Technology with threshold voltages for p and n-channel transistors of 0.6 volt. In this paper section II describes the implemented architecture of the amplifier and section III describes the architecture of the reference voltage. In section IV we discuss the simulation results and section V is the conclusion.

2. Design of the amplifier

The most important component in the design is the input stage. It requires a level shifting circuit too. The limited supply voltage restricts us to use single-transistor tail current source, which reduces CMRR. Alternative technique has been used to generate high impedance tail current from single transistor itself.

2.1 Input Stage

The main problem for designing the input stage is the limited supply voltage. Fig. 2 shows the comparison between the common-mode ranges with two different supply voltages. Contrary to the limited ICMR towards the supply rail this introduces a dead-zone in the middle of the supply range, where none of n-p complementary differential input pair operates. The vertically dashed section in Fig. 2 represents the compliance voltage for tail current source and the region with slanted lines represents the V_{gs} of the input transistors. These

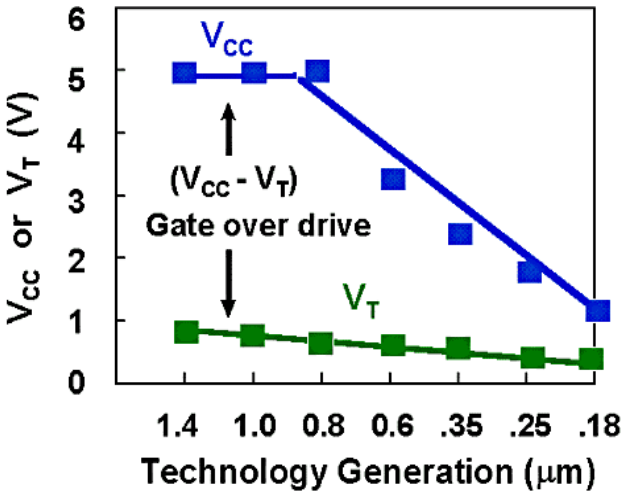

Fig. 1. Trend of supply voltage(V_{CC}) and threshold voltage(V_T) reduction with changing technology [2]. This shows the limitation in overdrive voltage available for analog design.

two voltages should remain almost same if we need to keep performance intact. Hence a dead-zone appears for low enough supply voltage.

The problem can be solved introducing different level-shifts to the input common-mode (V_{cm}) voltage such that, $V_{cm,n}$ and $V_{cm,p}$ received by n- and p-pair respectively, are different. These two voltages should ensure that complementary pair operates even within the dead-zone. The level-shift voltage (V_L) should be function of V_{cm} and must go down to zero

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towards the supply rails as either of the n-p complementary pair will automatically take over at that region. This requires a nonlinear nature of V_L as the current I_L shown in Fig. 4. The level-shift is obtained using resistors R_{L1}-R_{L4}, as shown in Fig. 3. I_L is the nonlinear current, also generated by the

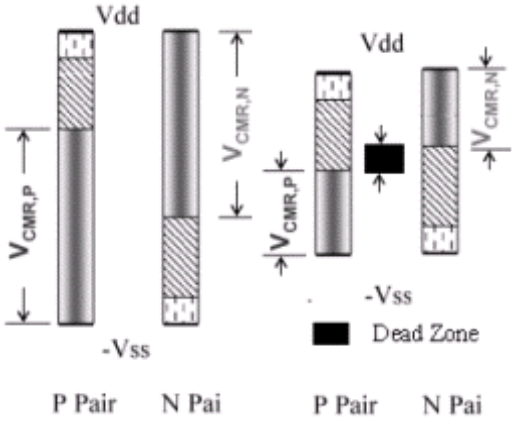

Fig. 2. The figure shows the available common-mode voltage for n- and p-differential pair.

common mode voltage to feed into these resistors (with help of current mirrors, M_{L1}-M_{L6}). This method, first used in BJT [3] and later also in CMOS is called a dynamic level shifting [4].

The input common mode voltages (Fig. 3) received by the n- and p-input differential pair are

$$V_{n,cm}=V_{cm} + I_L*R \quad \text{and} \quad V_{p,cm}=V_{cm} - I_L*R$$
$$V_{cm}= (V_{I+}+V_{I-})/2$$

where $V_{n,cm}$ and $V_{p,cm}$ are the common mode components of the input signal for n- and p-pair respectively. However very

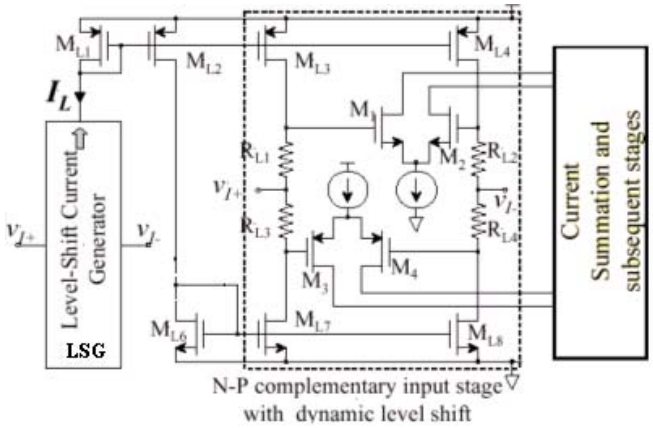

Fig. 3. The level shift current I_L driven through R_{L1-4} to generate input common mode voltages for n- and p-pair.

high matching between the input resistors should be ensured to have a high input impedance.

2.2 Level-Shift Current Generation

The shape of the nonlinear current is similar to that of the voltage V_L . This current can be generated by the tail currents of a similar complementary differential input stage. In conventional complementary differential pair, the tail currents of n- and p-pair(say, I_0 each) when added produces $2I_0$ when V_{cm} is at the middle of supply voltage. This is actually the cause of the g_m hump, which leads to instability of amplifier. On the contrary, for sub 1V supply the tail currents when added generate a shape similar to inverted I_L. This current when subtracted from a constant current produces the required I_L. The polarities of n- and p-tail currents should be made same before adding them such that they don't cancel each other. Hence the input voltage should be fed to both the

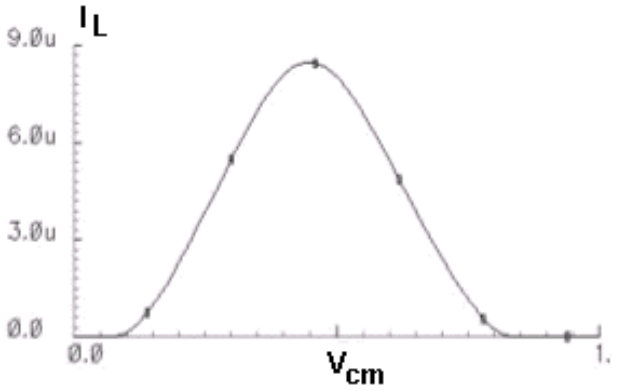

Fig. 4. Simulated output shows the required shape for the non-linear level shift current, I_L.

complementary input stage and also to the level shift circuit.

2.3 Current Summation Stage

The output current summation stage required for differential to single ended conversion usually does a folding (in folded cascade method) and mirroring of the four small signal currents. The conventional architecture uses the folding of both n- and p-differential currents on the same branch. This requires 4-stacked transistors with a minimum operating voltage of $V_t+3V_{ds,sat}$, leaving very little headroom available for signal swing. The alternative architecture is to use *different* branches for folding (for n- and p-differential currents) and having low-voltage current mirrors. This ensures a much greater signal swing at the output node.

2.4 High Impedance Tail Current Source

One of the important problems in the 1V amplifier is the low resistance of the single MOS tail current source. This leads to low CMRR value. The usual methods of increasing the resistance in tail current are, cascoding or using some source resistance for series-series feedback. Though both the method increases the resistance but at the same time increases the compliance voltage (V_{comp} , minimum voltage required for the current source). This is a major drawback for low voltage design. The method used in our circuit is a shunt-series

feedback [5] that increases the resistance like the previous cases but has a much lower V_{comp}. This method requires a high gain current-mode amplifier in the forward path and a feedback circuit basically of a current mirror with small but an accurate gain. This can be easily obtained in any amplifier

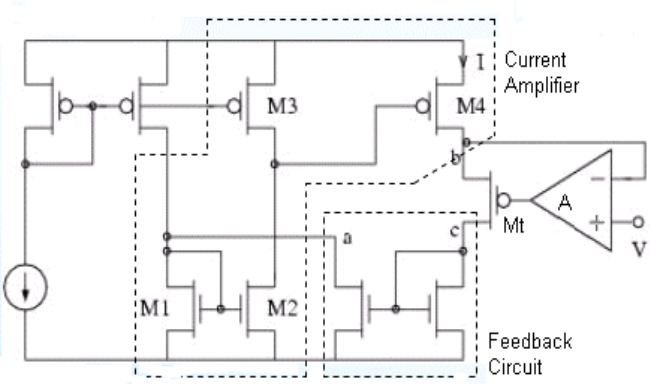

Fig. 5. Schematic of the circuit for testing the tail current source. M4 is the current source; Mt and amplifier A are used to fix the node voltage b externally.

circuit using the current mirror load (used in differential-to-single ended conversion stage), without any extra circuitry. The simplified schematic of the circuit is shown in Fig. 5. The high gain current amplifier (used in current mode designs) showed within dashed lines, consists M4 which is actually the high impedance tail current source. It can be observed that placing one of the differential input pairs within nodes b & c would form the basic amplifier structure itself. Current in feedback path should now have a 2:1 multiplier as one of the differential pair will carry only $I_{TAIL}/2$. The circuit was tested using Mt and an amplifier (A), which can vary the source potential of M4 so as to investigate its impedance and V_{comp}.

3. Bandgap Reference

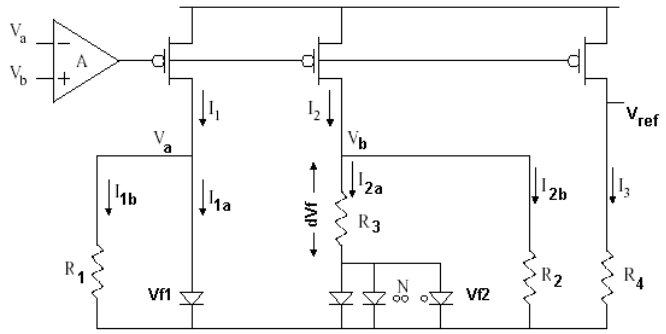

Fig. 6. Simplified schematic of the bandgap reference generator circuit. In practice R_1 and R_2 were made of two series resistors each, such that portion of V_a and V_b were fedback to the amplifier input.

The biasing circuit for this amplifier is of major importance. As the supply voltage available is only 1V, we cannot go for conventional bandgap reference circuits. The idea of bandgap reference is to add the negative temperature coefficient diode voltage (V_d) with the PTAT thermal voltage

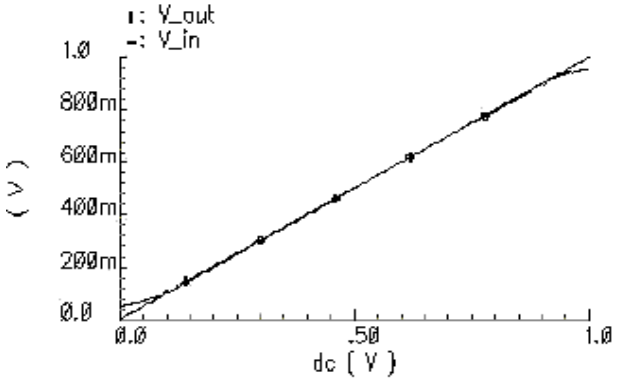

Fig. 7. Output of the amplifier in unity feedback mode. The ICMR is within 60mV from the supply rails.

(V_T), to generate a voltage (V_{BG}) independent of temperature. The value (V_{BG}) at which both the coefficients cancel each other is approximately 1.2V given by

$$V_{BG} = V_d + nV_T$$

Adding these two voltage terms in stack and using a current source to drive them, requires a minimum of 1.5V supply. This restricts the application of conventional bandgap reference circuit in 1V application. An alternative way is to generate currents proportional to these voltages and add them with proper multiplier. In this method we can achieve a fraction of the traditional bandgap voltage by scaling both the terms [6]. The restriction on supply voltage becomes much flexible.

The Fig. 6 shows a scheme of the circuit. The amplifier forces V_a and V_b to be equal and generates equal currents I_{1a} and I_{2a} as $R_1 = R_2$. We also see

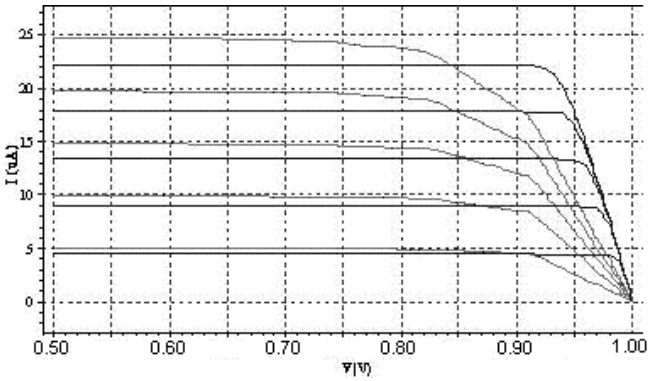

Fig. 8. Output impedance and $V_{compliance}$, tested for the tailcurrent source and a conventional cascaded current source.

$$I_{2a} = \frac{dV_f}{R_3}, I_{2b} = I_{1b} = \frac{V_{f1}}{R_2}$$

$$I_3 = I_2 = I_{2a} + I_{2b}$$

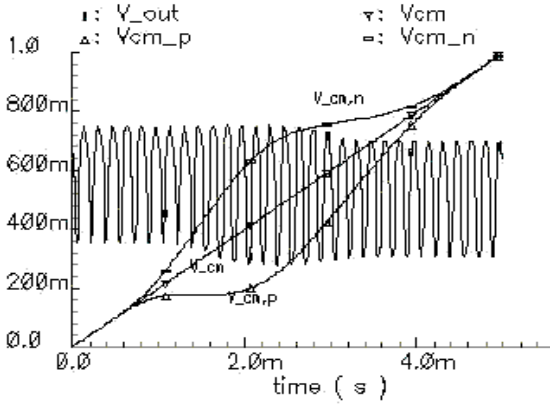

Fig. 9. Input common mode of the amplifier varied along with a very small differential voltage superimposed on it. The figure shows the open loop gain at different common mode voltage.

The reference output voltage is given by

$$V_{ref} = R_4\left(\frac{V_{f1}}{R_2} + \frac{dV_f}{R_3}\right) = \frac{R_4}{R_3}V_{ref,conventional}$$

Hence we can scale down the reference voltage according to our convenience. In the actual implementation of the circuit, design of the error amplifier is critical. It requires a high input common mode voltage (20

0mV around 700mV) and a low dc output voltage, to drive the pMOS. In order to have a more lenient input common mode swing, the voltages V_a and Vb were divided by resistive division and fed to the input of the amplifier. The bias current of the amplifier was also generated from the reference voltage itself. A separate startup circuit was used for proper functioning of the reference generator.

4. Simulation Results

All the circuits described above were designed at 0.35µ CMOS process. Rail-to-Rail ICMR of the amplifier being the

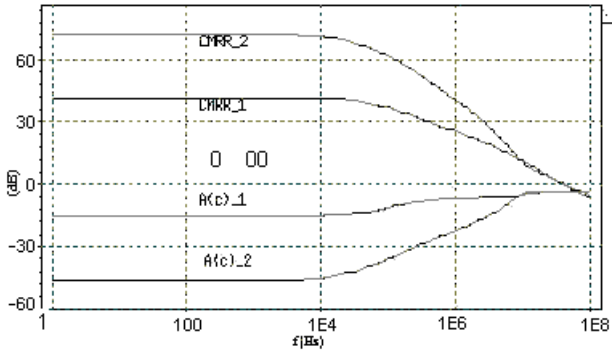

Fig. 10. The increase in CMRR in high impedance tail current source (CMRR_2) is due to the decrease in common mode gain A(c)_2.

main concern, no separate output stage was designed. DC gain without the output stage was 54dB. Load compensation of 1pF was used to stabilize the amplifier. The amplifier shows an input common mode range (tested in unity feedback

TABLE I
AMPLIFIER FEATURES

Quantity	Conversion from Gaussian and CGS EMU to SI [a]
Supply Voltage	1V
DC Gain (single stage)	54dB
GBW	1.3MHz
Phase Margin	65dB
Slew Rate	2V/µs
PSRR	64dB
CMRR	82dB
Noise Voltage$_{@500kHz}$	$40nV\sqrt{Hz}$
Power	250µW
Area	$0.130mm^2$

condition) within 50-60mV from the supply rails as shown in Fig. 7.

The common mode input voltage (Vcm, Fig. 9) was swept in open loop condition with a very small differential voltage superimposed on it. The Vcm_n, Vcm_p and the output voltage is shown in Fig. 8. The CMRR was improved from 40dB to 82dB using the high impedance tail current source. The curves in Fig. 9 shows a comparison between conventional cascoded current source and the one used here. The series-shunt feedback gives a much flatter output current along with low compliance voltage. The increase in CMRR is visible from Fig. 10 where A(c) represents the common mode gain. A decrease in A(c)_2 (with the high impedance tail) from A(c)_1 shows an increase in CMRR_2. The bandgap reference designed had a variation within 4mV for -20° to 100° temperature variation. The layout of the entire design (Fig. 11) took $0.13mm^2$. Other amplifier characteristics are given in Table I.

5. Conclusion

This paper presents a method of designing very low voltage (1 Volt) amplifier with full rail to rail to input CMR. These low voltage analog blocks will be essential for many applications like handsets in mobile communication. It is

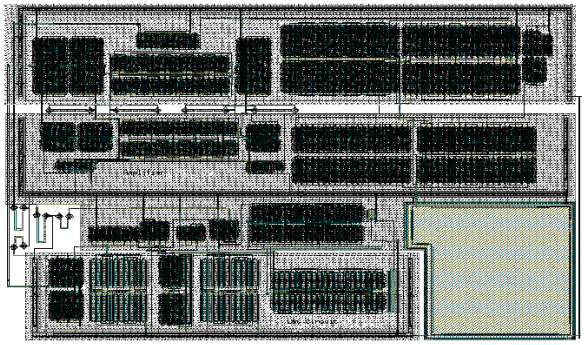

Fig. 11. The layout of the entire circuit covering $0.13mm^2$ area.

suggested through this work that current mode design is often suitable for such circuits as it reduces node voltage restrictions. A two-stage differential pair based Level -shifter

is suggested to get adaptive like tranconductance (g_m) control. This is essential for good stable operation of an amplifier. Finally we have shown that such an amplifier with features as given in table are achievable and its laid out to see its performance .

6. Acknowledgement

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