A VLSI Recurrent Network of Integrate-and-Fire Neurons Connected by Plastic Synapses With Long-Term Memory

Elisabetta Chicca, Davide Badoni, Vittorio Dante, Massimo D'Andreagiovanni, Gaetano Salina, Luciana Carota, Stefano Fusi, and Paolo Del Giudice

***Abstract*—Electronic neuromorphic devices with on-chip, on-line learning should be able to modify quickly the synaptic couplings to acquire information about new patterns to be stored (synaptic plasticity) and, at the same time, preserve this information on very long time scales (synaptic stability). Here, we illustrate the electronic implementation of a simple solution to this *stability-plasticity problem*, recently proposed and studied in various contexts. It is based on the observation that reducing the analog depth of the synapses to the extreme (bistable synapses) does not necessarily disrupt the performance of the device as an associative memory, provided that 1) the number of neurons is large enough; 2) the transitions between stable synaptic states are stochastic; and 3) learning is slow. The drastic reduction of the analog depth of the synaptic variable also makes this solution appealing from the point of view of electronic implementation and offers a simple methodological alternative to the technological solution based on floating gates. We describe the full custom analog very large-scale integration (VLSI) realization of a small network of integrate-and-fire neurons connected by bistable deterministic plastic synapses which can implement the idea of stochastic learning. In the absence of stimuli, the memory is preserved indefinitely. During the stimulation the synapse undergoes quick temporary changes through the activities of the pre- and postsynaptic neurons; those changes stochastically result in a long-term modification of the synaptic efficacy. The intentionally disordered pattern of connectivity allows the system to generate a randomness suited to drive the stochastic selection mechanism. We check by a suitable stimulation protocol that the stochastic synaptic plasticity produces the expected pattern of potentiation and depression in the electronic network. The proposed implementation requires only 69×83 $\mu\mathrm{m}^2$ for the neuron and 68×47 $\mu\mathrm{m}^2$ for the synapse (using a 0.6 μm, three metals, CMOS technology) and, hence, it is particularly suitable for the integration of a large number of plastic synapses on a single chip.**

***Index Terms*—Integrate-and-fire neurons, learning systems, neuromorphic aVLSI, synaptic plasticity.**

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I. Introduction

ONE of the main obstacles that hindered the development of neuromorphic analog systems is the lack of a reliable, robust, and simple implementation of a *learning* mechanism, with the associated need of a suitable synaptic device. Difficulties range from the choice of the synaptic (and learning) model, both as to the biological and the computational appeal, to the design of the electronic device implementing the synapse and its learning dynamics. In particular, the synapse has to cope with the need of *long-term* storage, coupled to a *quick* ability to modify its state depending on instantaneous changes in the environment, to effect the learning mechanism.

The combination of digital memories and digital-to-analog converters is not really an option for the integration of large scale neuromorphic networks. Hence, in the past, and still now, one of the favorite solutions for the problem of long-term storage relies on floating gates (see, e.g., [4], [5] and references therein).

Recently proposed models of synaptic dynamics [1] suggest a possible and effective alternative to the solution offered by floating gates. A network of neurons can perform well as an associative memory even if the analog depth of the synapses is reduced to the extreme (two stable states on long time scales). Scenarios with binary or multistable synapses explored in the past (see, e.g., [6]) usually comprised a first stage in which the structure of the patterns is stored in analog synapses. Only in the end, after all the patterns to be stored have been presented to the network, the analog synapses, are clipped to one of the discrete stable states. In case of online learning in realistic conditions, this approach is not possible: With binary or multistable synapses the new patterns overwrite the information about the old ones and the forgetting process is too fast to permit any classification [7], [8]. The solution is to change only a small fraction of synapses when patterns are presented to be learned. The price to be paid is that the patterns should be presented more than one time and learning is slow. A possible unbiased, local mechanism which would select a given fraction of synapses is stochastic learning: At parity of pre- and postsynaptic activities, each synapse makes a transition with some probability. This mechanism guarantees that in average the same fraction of synapses changes upon presentation of a given stimulus. Provided that the transition probabilities are small enough, this stochastic selection allows to recover optimal performances in terms of storage capacity [7].

This approach moves the problem to the generation of the appropriate stochastic process which would provide the needed random selection. Generating rare events in a material device like an electronic synapse is a difficult problem and usually requires either bulky devices, like big capacitors, or fine-tuning of the currents which control the dynamics. Moreover, the analog noise generated by analog devices is rather sensitive to temperature and humidity. The solution proposed in [1] exploits the irregularity of the neuronal activity, which in turn emerges as a collective property of the network interactions when the pattern of connectivity is intentionally disordered [2], [3]. In particular, the synapse discussed in this paper is designed to encode the mean firing rates of the pre- and postsynaptic neurons. In this specific case, the interspike variability can be exploited to have stochastic transition between stable states at parity of mean firing rates.

The above scenario for the synaptic dynamics relies on *spike-driven* modifications, which bring us to the adopted neuron model: the integrate-and-fire neuron. This leaves out easier, but poorer, solutions, based on an effective representation of the spiking neural activity (as in the case of neurons implemented through their *transfer function*). Thus, when online, dynamic learning is the goal, spiking neurons are not only an option for biological plausibility but are a computational need.

II. Hardware Implementation

We present a very large-scale integration (VLSI) recurrent network implemented on a 3.16×3.16 mm^2 standard 0.6 μm three-metals CMOS technology chip (see Fig.1). It contains 21 integrate-and-fire neurons (14 excitatory and seven inhibitory) randomly interconnected by 129 synapses (connectivity 30%). The 56 synapses between excitatory neurons are plastic; all the others are fixed. The plastic synapses are designed to implement a covariance based learning rule: When the mean spike frequencies of the pre- and postsynaptic neurons are high, the synapse is potentiated with some probability. In case of a mismatched pair of activity (the presynaptic neuron fires at high rate, while the postsynaptic neuron is silent) the synapse is depressed with another probability. No transitions occur for low presynaptic activity. Although the synapse has been designed to read and encode mean spike frequencies, the synaptic dynamics is also sensitive to higher order statistics and to the correlations of the pre- and postsynaptic spike trains. The synaptic state, which can be potentiated or depressed, determines the excitatory postsynaptic current (EPSC), generated by the synaptic circuit when a presynaptic spike is emitted.

The nonplastic synapses simply implements the post-synaptic current injection (excitatory and inhibitory). The disorder intentionally introduced in the pattern of connectivity plays an important role in making the network activity irregular (see Section III).

A. Neuron

The main building blocks of the network are simple integrate-and-fire electronic neurons with constant leak, functionally equivalent to those described in [9]. These neurons integrate linearly the total afferent current and when a threshold is crossed they emit a spike. The subthreshold dynamics can be described by the equation governing the voltage across a capacitor (which represents the membrane potential of the cell)

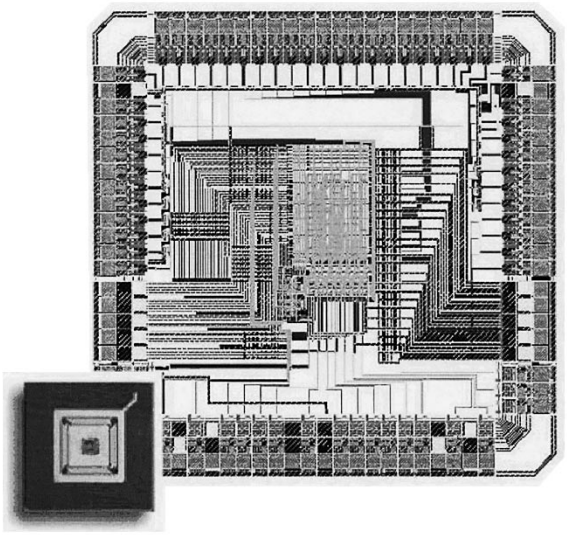


Fig. 1. Layout of the chip. It is a 3.16×3.16 mm^2 chip implemented using standard 0.6 μm three-metal CMOS technology.

$$V_{\text{soma}}(t) = V_{\text{soma}}(0) - \frac{1}{C} I_\beta(t) t + \frac{1}{C} \int_{t_0}^{t} I(t') dt' \quad (1)$$

where $I(t)$ is the sum of the excitatory external current and all excitatory and inhibitory presynaptic currents, I_β is the leak current, and C is the soma capacitance. As V_{soma} crosses the threshold θ, a spike is emitted and the membrane potential is reset to V_{reset}. Equation (1) must be complemented by the condition that V_{soma} cannot go below a minimal value V_{rest} which represents also the resting potential of the neuron. This rigid barrier turned out to be essential to achieve a qualitatively similar behavior to the one of the integrate-and-fire neuron with a leakage proportional to the membrane potential [10].

A schematic diagram of the circuit implementing the neuronal dynamics is shown in Fig. 2. Transistors M1–M4 and capacitors C1–C2 implement the dynamics described by (1). The circuit can be divided in four functional blocks.

1) *Input Block.* The total dendritic input current $I(t) = I_{\text{exc}} - I_{\text{inh}}$ is injected into the soma capacitance $C = C1 + C2$ through transistors *M*1 and *M*2, which act as digital switches. They are required to interrupt the current flow when the neuron is emitting a spike and to guarantee that the spike duration is not dependent on the input current.
2) *Leak Block.* The leak current I_β is set by the bias voltage V_β (transistor *M*3) and it is turned off during the emission of a spike (*M*4 acts as a digital switch) such that the duration of the spike acts effectively as an absolute refractory period.
3) *Action Potential Block.* Transistors *M*5–*M*6, capacitors *C*1–*C*2 and inverters *N*1–*N*2 implement the spike emission mechanism. The input current is integrated by the parallel of the two capacitors *C*1 and *C*2. As

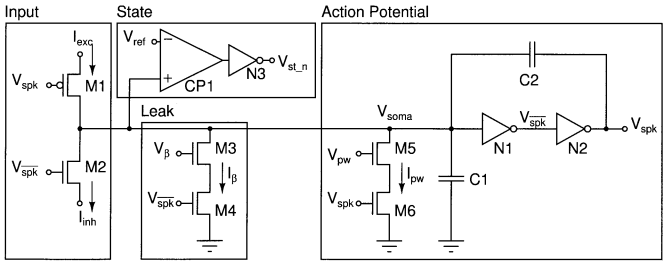


Fig. 2. Schematic diagram of the integrate-and-fire neuron. The four functional blocks (input, state, leak, and action potential) implement an integrate-and-fire neuron which integrates linearly the input, has a constant leakage, and emits a spike when $V_{\rm soma}$ crosses a threshold. See the text for a detailed description.

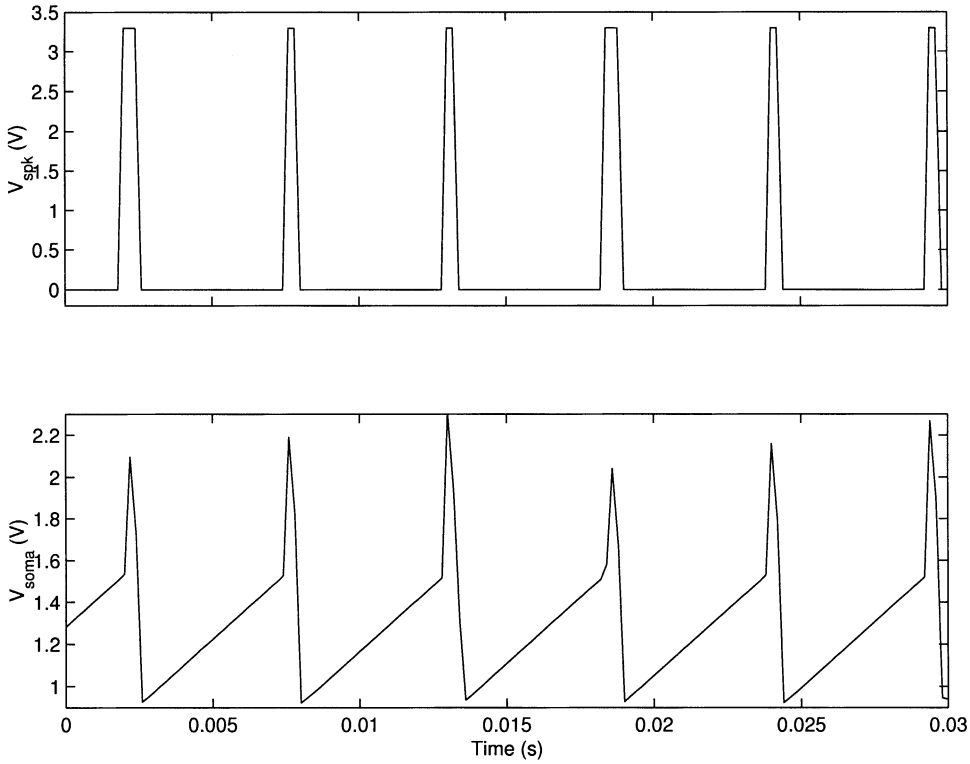


Fig. 3. Neuronal dynamics. The neuron integrates linearly a constant current. As soon as $V_{\rm soma}$ (bottom trace) crosses the threshold θ for emitting a spike, the action potential is initiated, and an impulse (top trace) is generated by the spike emission block. A positive feedback loop drives $V_{\rm soma}$ to $\theta + V_{dd}C_2/(C_1 + C_2)$ from which $V_{\rm soma}$ decays linearly, down to θ. As $V_{\rm soma}$ crosses θ from above, the output voltage $V_{\rm spk}$ goes back to the ground level (spike inactivation), and the membrane potential decreases by a fixed amount.

$V_{\rm soma}$ crosses from below the switching voltage $V1$ of the inverter *N*1, the output voltage $V_{\rm spk}$ rises from ground to the positive power supply rail V_{dd} (spike activation). A positive feedback loop, implemented by the capacitive divider *C*1–*C*2, increases $V_{\rm soma}$ by $V_{dd}C2/(C1 + C2)$[9]. As long as $V_{\rm spk}$ is equal to V_{dd}, the digital switch *M*6 is closed, and the current set by the bias voltage V_{pw} can discharge the two capacitors causing the membrane potential to decay linearly. As $V_{\rm soma}$ crosses again (this time from above), the switching voltage $V1$ of the inverter *N*1, the output voltage $V_{\rm spk}$ goes back to the ground level (spike inactivation), and the membrane potential decreases by $V_{dd}C2/(C1 + C2)$ because of the action of the positive feedback loop. The integration of the input current can then start again.

4) *State Block.* Upon the presentation of a presynaptic spike the plastic synapses tend to be potentiated/depressed if the postsynaptic membrane potential is above/below a certain threshold ($V_{\rm ref}$). A digital signal (V_{st_n}) is generated to encode the state of the neuron ($V_{\rm soma}$ below or above $V_{\rm ref}$). This function is implemented with comparator *CP*1 and inverter *N*3.

The spike duration (τ_0) can be modified by changing the current I_{pw}, and the interval between two consecutive spikes (ΔT) depends on the input currents ($I_{\rm exc}$ and $I_{\rm inh}$) and on the leak current (I_β). This characteristic times, and then the spike rate, can be easily calculated in the simple case of constant and positive $I_{\rm exc} - I_{\rm inh} - I_\beta$. ΔT is the time needed to the membrane potential to reach the switching voltage of inverter *N*1 ($V_{dd}/2$) starting from the reset potential ($V_{dd}/2 - VddC2/(C1 + C2)$)

$$\Delta T = V_{dd}\frac{C2}{I_{\rm exc} - I_{\rm inh} - I_\beta}. \tag{2}$$

The spike duration is given by

$$\tau_0 = V_{dd}\frac{C2}{I_{pw}}. \tag{3}$$

In this case, $V_{\rm soma}$ is a periodic signal with period

$$T = \Delta T + \tau_0 = V_{dd}C2\left(\frac{1}{I_{\rm exc} - I_{\rm inh} - I_\beta} + \frac{1}{I_{pw}}\right) \tag{4}$$

where $C1 = 377$ fF, $C2 = 375$ fF, $Vdd = 3.3$ V. An acquisition of the dynamic of the neurons in this simple case is shown in Fig. 3. A small hysteresis (about 50 mV) in the switching voltage of the inverter $N1$ affects the spike activation and inactivation thresholds. This hysteresis is due to two sources of nonideality of the inverter: the differences between PMOS and NMOS transistor parameters, and the presence of parasitic capacitances. The order of magnitude of the measured hysteresis is compatible with Spectre simulation results for the neural circuit including the parasitic capacitances extracted from the layout.

During the design of the layout, particular attention was given to prevent possible problems due to the coexistence, on the chip, of fast varying signals (like $V_{\rm spk}$) and slow analog signals (like $V_{\rm soma}$). Parasitic capacitances between those signals can cause cross-talk, inducing undesired changes in the analog signal when the fast varying signal changes. To minimize the parasitic capacitances, and then prevent to the cross-talk, a layer of metal, connected to the positive power supply rail or to ground, was inserted (wherever possible) between the crossing of two wires (on different layers) connected to different nodes of the circuit.

The layout of the neuron circuit covers an area of about 69×83 μm^2 (see[8] for more details).

B. Plastic Synapse

The excitatory neurons are connected by plastic synapses. Their dynamics is described in terms of a single internal variable ($V_{\rm syn}$), which represents the voltage across a capacitor. The synaptic efficacy depends on this internal state variable as explained below. Although $V_{\rm syn}$ is inherently analog, the synapse is designed in such a way that only the maximum and the minimum allowable values of $V_{\rm syn}$ are stable on long time scales, in the absence of presynaptic neuronal activity. Indeed, when $V_{\rm syn}$ is above some threshold $V_{\rm thr}$, a positive current drives $V_{\rm syn}$ to the upper bound (V_{dd}); otherwise, the synaptic capacitor is discharged at a regular pace until $V_{\rm syn}$ hits the lower bound (0 V). These two values are then preserved indefinitely and survive also in the presence of small fluctuations which do not bring $V_{\rm syn}$ across the threshold $V_{\rm thr}$. This bistability preserves the memory of one of the two states on long time scales and, hence, we will refer to the two currents described above as to the *refresh* currents. Upon the arrival of a presynaptic spike, the internal state of the synapse is modified to acquire information about the neuronal activity and, hence, about the stimulus. If the postsynaptic depolarization is above some threshold $V_{\rm ref}$ (see description of the *State Block* in Section II-A), the internal state $V_{\rm syn}$ is pushed upwards; otherwise, it is pushed downwards. If these temporary changes accumulate and bring $V_{\rm syn}$ across the threshold $V_{\rm thr}$, the synapse is then attracted toward a different stable state, and a transition occurs. As a consequence the role of the synaptic threshold is at least twofold: On one hand it separates two bands of synaptic values which are the basins of attraction for two stable memory values; on the other hand, it provides a simple and automatic mechanism to select only a fraction of synapses which would undergo a permanent change during the presentation of a stimulus. If the neuronal activity is irregular, then this selection mechanism is stochastic and implements the mechanism needed to recover the optimal performances of the networks as an associative memory (see also Section V). The specific form of the temporary changes induced by the neuronal activity has been designed to encode the mean spike rates of the pre- and postsynaptic neurons. The presynaptic activity acts as a trigger (no transition can occur in case of low presynaptic spike frequency) and, then, the direction of the change is determined by the depolarization of the postsynaptic neuron. The latter provides a simple and instantaneous way to read indirectly the postsynaptic mean firing rate (see [1]).

The circuit implementing the described dynamics can be divided into five functional blocks [see Figs. 4 and 5(a)].

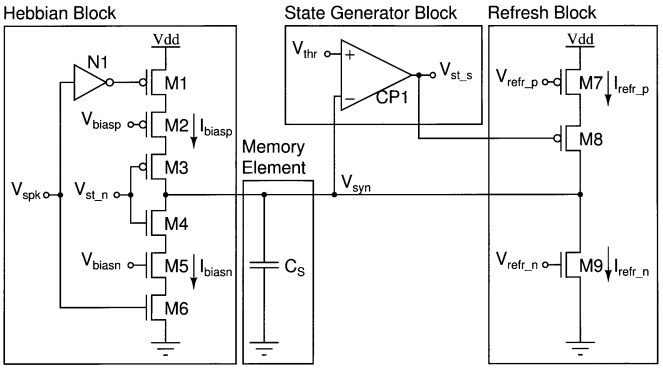


Fig. 4. Schematic diagram of the plastic synapse. The internal state of the synapse is determined by the voltage across capacitor C_s. The state generator block and the refresh block ensure the preservation of memory on long time scales. The Hebbian block contains all the information about the learning prescription. See the text for more details.

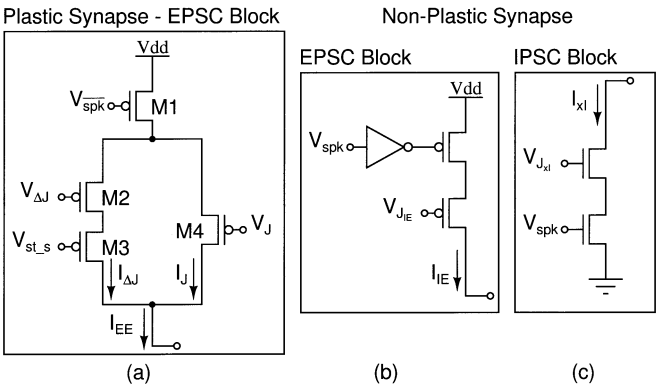


Fig. 5. (a) Schematic diagram of the EPSC block of the plastic synapse. V_{st_S} is a digital voltage representing the synaptic state (potentiated or depressed). An EPSC is generated only upon arrival of a presynaptic spike. The output current is $I_{\rm exc} = I_J$ when the synapse is depressed state and $I_{\rm exc} = I_J + I_{\Delta J}$ when it is potentiated. Both I_J and $I_{\Delta J}$ are set externally. (b) Nonplastic excitatory synapse circuit. When a presynaptic spike occurs, the current $I_{\rm IE}$ (externally set) is injected in the postsynaptic capacitance. (c) Nonplastic excitatory synapse circuit. An IPSC of intensity I_{xI} ($x \in \{E, I\}$, both currents are externally set) is generated upon arrival of a presynaptic spike.

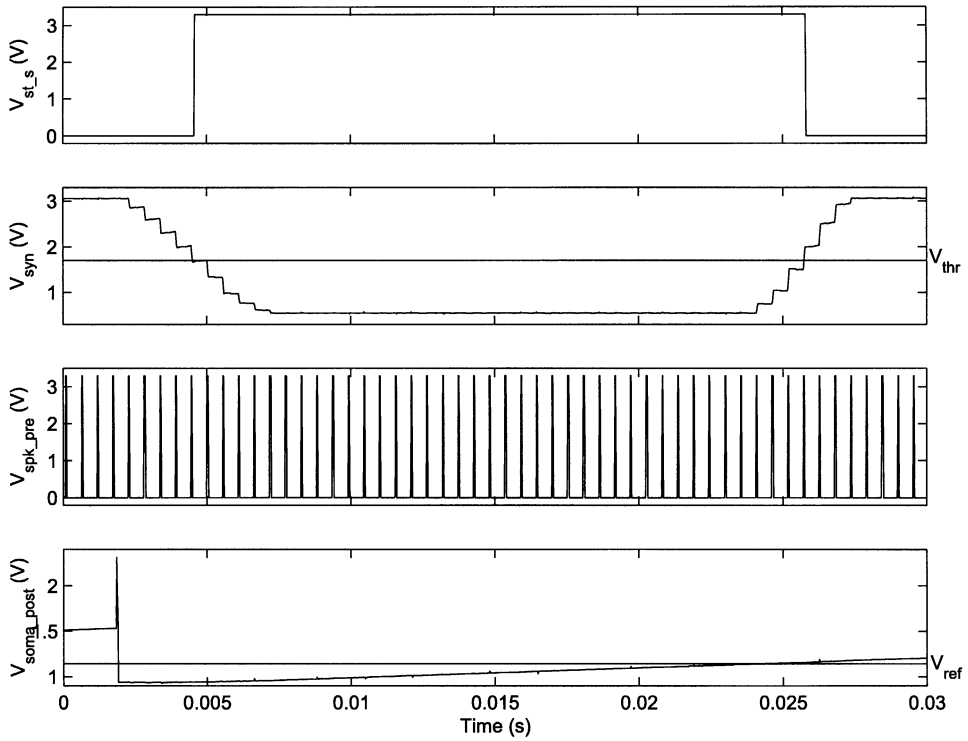


Fig. 6. Synaptic dynamics is illustrated by showing the oscilloscope acquisition of the following signals (from top to bottom). Digital synaptic state (V_{st_s}), analog synaptic variable ($V_{\rm syn}$), presynaptic input spike ($V_{\rm spk}$), postsynaptic membrane potential. The presynaptic and postsynaptic neurons are injected a constant current which brings them at the spike threshold at a regular pace (high frequency for the presynaptic neuron and low frequency for the postsynaptic one). The synapse state starts from the lowest bound (potentiated state) and is then pushed up by a succession of presynaptic spikes which find the membrane potential of the postsynaptic neuron below $V_{\rm ref}$. As soon as $V_{\rm syn}$ crosses the synaptic threshold $V_{\rm thr}$, the synapse is attracted toward the depressed state ($V_{st\_s} = V_{dd}$). A series of upward jumps induced by presynaptic spikes which occur in coincidence with high post-synaptic depolarization brings $V_{\rm syn}$ above the threshold again. Note that the topmost trace, which represents the digital synaptic state, and hence, the real synaptic efficacy, is either zero or V_{dd}, depending on whether $V_{\rm syn}$ is above or below the synaptic threshold $V_{\rm thr}$.

1) *Memory element*. The analog variable of the synapse V_{syn} is stored using a capacitor ($C_S = 327$ fF).
2) *State generator block*. A digital signal (V_{st_s}), representing the state of the synapse (potentiated or depressed), is generated by the comparator *CP*1. V_{st_s} is the input signal for the *refresh block* discussed in 3) and the excitatory postsynaptic current (EPSC) block discussed in 5). If the voltage representing the internal variable of the synapse is greater/less than the threshold voltage V_{thr}, the digital signal V_{st_s} is low/high, and the synapse is potentiated/depressed. In fact, in the EPSC block, V_{st_s} determines the intensity of the current injected in the postsynaptic neuron upon presentation of a presynaptic spike and, hence, it determines the synaptic efficacy.
3) *Refresh block*. When the presynaptic neuron is inactive the synapse has to maintain the state generated by the previous stimulations. The transistors *M*7–*M*9 implement this function. When the synapse is depressed ($V_{st\_s} = V_{dd}$) its state is maintained by means of the current I_{refr_n}. When the synapse is potentiated ($V_{st\_s} = 0$ V), the current injected into the synaptic capacitor is given by the difference $I_{refr\_p} - I_{refr\_n}$, which has to be positive to maintain the potentiated state. We have to set $I_{refr\_p} = 2I_{refr\_n}$ to have an equal amount of positive and negative refresh currents.
4) *Hebbian block*. Transistors *M*1–*M*6 and inverter *N*1 implement the Hebbian block. Transistors *M*1 and *M*6 act as digital switches and the current can flow only when a presynaptic spike is active. The sign of the current is determined by the postsynaptic digital signal V_{st_n} through the switches *M*3 and *M*4. If V_{st_n} is low (the membrane potential of the postsynaptic neuron is greater than $V_{\rm ref}$), the current $I_{\rm biasp}$ charges the synaptic capacitor and it tends to potentiate the synapse. If V_{st_n} is high (the membrane potential of the postsynaptic neuron is less than $V_{\rm ref}$), the current $I_{\rm biasn}$ discharges the synaptic capacitor and tends to depress the synapse.
5) *EPSC block*. The schematic diagram of the EPSC is shown in Fig. 5(a). The synaptic current is injected into the postsynaptic soma capacitor only upon the occurrence of a presynaptic spike (transistor *M*1 acts as digital switch). If V_{st_s} is high, the digital switch implemented by transistor *M*3 is open, and the EPSC $I_{\rm EE}$ is given by $I_{J\_} = I_J$ (depressed synapse). The current I_J is set by the bias voltage V_J. If V_{st_s} is low, transistor *M*3 is closed, and the EPSC $I_{\rm EE}$ is equal to $I_{J+} = I_J + I_{\Delta J}$ (synapse potentiated). The current $I_{\Delta J}$ is set by the bias voltage $V_{\Delta J}$. The total excitatory afferent current to the neuron (I_{exc}) is the sum of all the I_{EE} contributions, plus possible external currents.

The layout of the synaptic circuit covers an area of about $68 \times 47\ \mu{\rm m}^2$.

Fig. 6 shows a time record example of the synaptic internal state variable (trace 2) and the synaptic state (trace 1) of an ex-

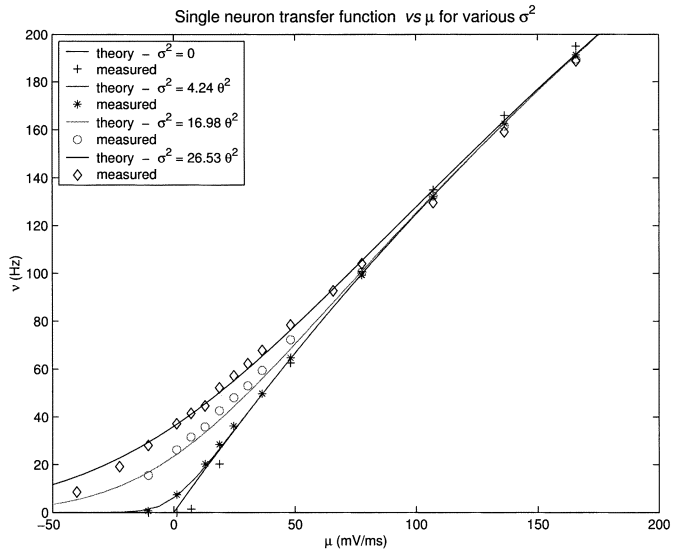


Fig. 7. Neurons transfer function: The mean frequency as a function of the mean μ and the variance σ^2 of the input current. Each curve represents the predicted firing rate as a function of μ of the current for a specific σ^2. The corresponding measured spike frequencies are indicated by various symbols (diamonds, circles, stars, and crosses).

citatory synapse, with the associated time course of the presynaptic spike train (trace 3) and postsynaptic membrane potential (trace 4).

C. Nonplastic Synapse

The nonplastic synapse is implemented with a circuit that injects a fix amount of charge in the postsynaptic membrane capacitance upon presentation of a presynaptic spike. It is a simple EPSC or inhibitory PSC (IPSC) block with only one possible value for the output current. The schematic diagrams of the excitatory and inhibitory nonplastic synapse are shown in Fig. 5(b)–(c), where I_{IE} is the EPSC set by the bias voltage $V_{J_{IE}}$ and I_{xI} ($x \in \{E, I\}$) are the IPSC set by the bias voltage $V_{J_{xI}}$

D. Test Setup

Extensively testing the electronic neurons and synapses is an important complement to exploring the dynamic collective behavior of the implemented recurrent neural network (such results are reported in [2] and [11]). A programmable setup has been designed and built. This setup, besides allowing basic chip parameters setting, enables reliable injection of currents with the desired statistical properties in the neurons on the chip and real-time acquisition of the spikes emitted by the neurons.

The analog VLSI network is hosted by a reconfigurable microcontrolled I–O board that provides the control parameters, the static network parameters, and the input external current via 12 bit multifunction DAC modules. Output spikes are gathered by another micro-controlled device (the acquisition board) endowed with 64 Kspikes total memory on board; for example, a 50-Hz rate implies about 60 s of available time span for recording the neuron's activity. Each spike is encoded as the label of the emitting neuron and the attached time label. A workstation handles the communication with the I–O board. A high-level user interface has been developed for parameters setting, spikes recording, and data visualization and analysis.

To characterize the input–output properties of the single neuron receiving noisy afferent currents, we needed a controlled source of external noise to inject into the neuron. For this purpose, a suitable off-chip generator of pseudorandom current signals was designed and built. The noise generator is based on a classical scheme exploiting the properties of feedback shift registers [12], [13]. The output digital waveforms are usually filtered (e.g., by an RC low-pass circuit) to produce an analog Gaussian noise signal, while in this case, the integrate-and–fire neuron itself provides the filter acting as an integrator.

III. Single Neuron and the Network

In order to characterize the dynamic response of the single neuron receiving input current with various statistical properties, some parameters must be estimated first.

A. Leakage I_β

The leakage term I_β^i is estimated for each neuron i, for a set of values of the global parameter I_β which controls I_β^i, in order to check the linearity of I_β^i versus I_β in the range of interest.

I_β^i is simply derived by comparing the slopes of the neuron's depolarization upon injecting a dc external current with and without the leakage term.

While I_β^i is pretty linear for all neurons for $I_\beta \in [0, 0.2]\ \mu$A, the slope of the fit has a significant spread among the neurons, apparently due to a high variability in the mirrored I_β^i currents.

The measured values for the slope b of the linear fit have mean equal to 5.32 and variance equal to 0.86.

B. Time Width of the Spike

The time duration τ_0 of the spike has been directly measured on the oscilloscope, for an interval of values of $I_{pw} \in [0, 2]\ \mu$A. The linear fit gives $(1/\tau_0) = 10^{-5} \cdot I_{pw} - 10^{-4}$ ms; $r^2 = 0.9996$.

C. Single Neuron Current-to-Rate Transfer Function

To characterize the response properties of the implemented neuron for noisy input currents we adopted the following procedure.

- The feedback shift-register random generator mentioned in Section II-D generates sequences mimicking a binomial process to produce a random switching signal between preset "high" and "low" values ("random period square wave").
- The mean and variance of the random simulated current signal are computed as

$$\mu = \frac{\Delta V_+ - \Delta V_-}{2T}$$
$$\sigma^2 = \frac{(\Delta V_+ + \Delta V_-)^2}{4T}$$

  where ΔV_+ and ΔV_- are the voltage jumps in the neuron's potential which are induced in a clock period T of the noise generator.
- The computed mean and variance are plugged into the theoretical formula of the neuron's transfer function [10]

$$\nu = \Phi(\mu, \sigma) = \left[\tau_0 + \frac{\sigma^2}{2\mu^2}\left(e^{-(2\mu\theta/\sigma^2)} - e^{-(2\mu V_{\rm reset}/\sigma^2)}\right) + \frac{\theta - V_{\rm reset}}{\mu}\right]^{-1}$$

  where ν is the spike frequency of the neuron, θ is the spike emission threshold, and $V_{\rm reset}$ is the reset membrane potential. All other relevant parameters ($\theta, V_{\rm reset}, \tau_0, I_\beta$) are independently measured as reported above.
- The experimental transfer function is checked against the theoretical predictions.

Fig. 7 shows that theoretical predictions are fairly well matched by the measured neuron response. This current-to-rate transfer function contains all the single neurons properties that are relevant to the network collective dynamics in stationary conditions [10].

D. Neurons Coupled by Excitatory Connections

We briefly sketch in the following few relevant features exhibited by the interacting network (further details in [2], [3], and [11])

Our intention is to show a glimpse of the rich phenomenology exhibited by such a small electronic network, in view of the scenario outlined in the Introduction, which envisages the recurrent neural activity providing a dynamic source of randomness to be exploited by the synapses to implement stochastic, slow modifications of the efficacies.

We remark that each synapse evolves on the basis of information which is local in time and space (the instantaneous activities of its pre- and postsynaptic neurons); the high feedback in the network makes the activity of each neuron able to reflect any sources of disorder, first of all in the pattern of connectivity, which is fixed but random in our case.

1) Excitatory-to-Excitatory Synapse: We call in the following J_{xy} ($x, y \in \{E, I\}$) the EPSC or IPSC induced by the four possible types of synaptic couplings between excitatory and inhibitory neurons.

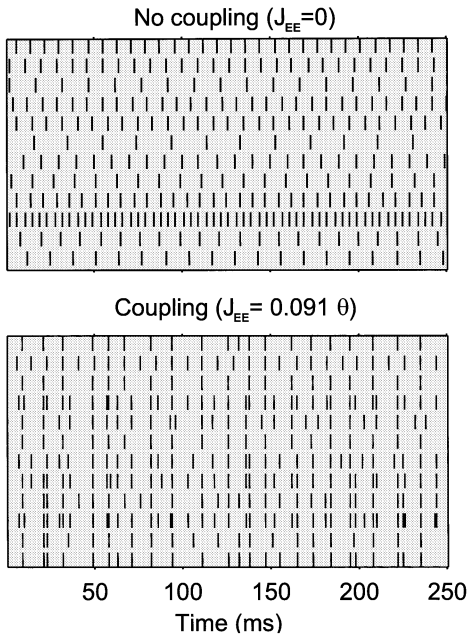


Fig. 8. Raster plots of the spikes produced by the network for two different external currents (each tick mark corresponds to a spike and each row contains a different excitatory neuron). The same current is injected to all the excitatory neurons. Top: The neurons are decoupled (the synaptic efficacies are set to zero) and fire very regularly, indicating that the electronic noise is negligible. Bottom: The excitatory interactions are turned on, and the external current is reduced in order to get the same mean spike frequency. The neurons now feel the disorder intentionally introduced in connectivity pattern, and they fire more irregularly. This is the randomness which drives the stochastic selection mechanism.

As a preliminary step, we set $I_J \neq 0$ and $I_{\Delta J} = 0$; the effective value of the excitatory-to–excitatory synaptic efficacy $J_{\rm EE}$ versus the global parameter I_J has been directly measured, by measuring the jumps ΔV induced in the potential of the postsynaptic neuron by spikes emitted by the presynaptic neuron.

$\Delta V/\theta = 5 \cdot 10^{-5} I_J - 0.0027$ mV; $r^2 = 0.992$ for $I_J \in [0, 4]$ μA.

2) Deterministic Excitatory Network: Fig. 8 shows two *raster* representations of the network activity for uncoupled neurons (all the synaptic efficacies are set to 0, top) and for neurons coupled by excitatory synapses ($J_{\rm EE} \neq 0$, $J_{\rm EI} = J_{\rm IE} = J_{\rm II} = 0$, bottom). The spikes emitted by each neuron are represented by drawing a bar at the corresponding position along the time axis; each row in the raster represents a sequence of spikes emitted by a given neuron (rasters of this kind are a common representation of the neural activity in experimental neuroscience).

The top panel in Fig. 8 illustrates a situation in which the same (constant and positive) input current is set for all the uncoupled neurons. Because of the various inhomogeneities (in the current mirrors, in the neurons themselves) the neurons exhibit a wide variability in the firing rate (though we remark that the firing of any given neuron is quite stable and reproducible).

Excitatory synaptic couplings are switched on in the bottom panel (the synaptic dynamics is not active), while the input current is still constant and equal for all neurons; its value is adjusted in order to compensate for the mutual excitation and to

have the same average firing rate. It is clearly seen that, despite the fact that no additional source of randomness has been introduced, the recurrent excitation through a disordered pattern of connectivity is enough to endow the neurons' firing pattern with high variability.

This qualitative observation can be put on quantitative basis by making contact with the *mean field* predictions appropriate for the given network architecture; detailed checks have been carried out, which provide, for the toy external stimulation examined, a surprisingly good match between mean field predictions and the behavior of such a small network [2], [11].

IV. Synaptic Plasticity in a Network Setting: Learning a Pattern

We moved next to investigate how the plasticity of the electronic synapses shows up in a network environment.

In [1], it was proven that the synaptic device described in Section II-B implements a stochastic Hebbian mechanism by studying a single externally driven synapse.

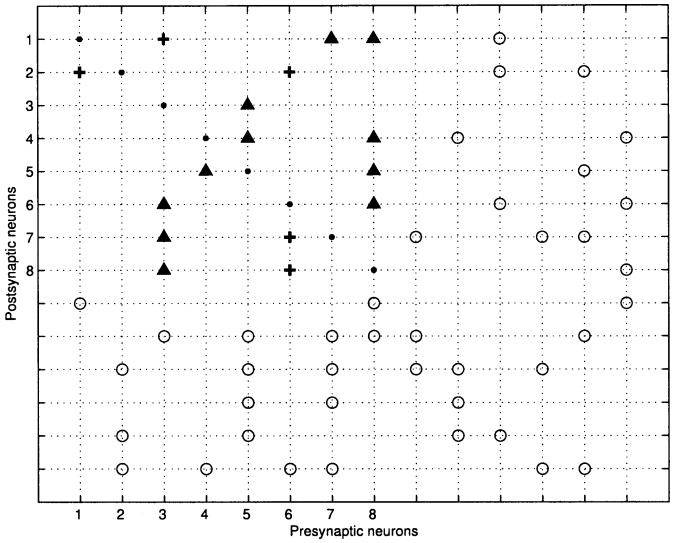
Specifically, the probability of potentiation ($V_{\rm syn}$ crosses $V_{\rm thr}$ from below, the efficacy—postsynaptic current—goes from I_{J-} to $I_{J+} = I_{J-} + I_{\Delta J}$) is high for highly active pre- and postsynaptic neurons; in this condition one has a negligible probability of synaptic "depression." The latter dominates when the synapse has a high presynaptic activity but a poorly activated postsynaptic neuron. Transition probabilities are effectively suppressed in both directions when the presynaptic neuron has low activation.

In [3], it was shown how the noise globally generated by the network allows control of a wide range of transition probabilities for the synaptic device.

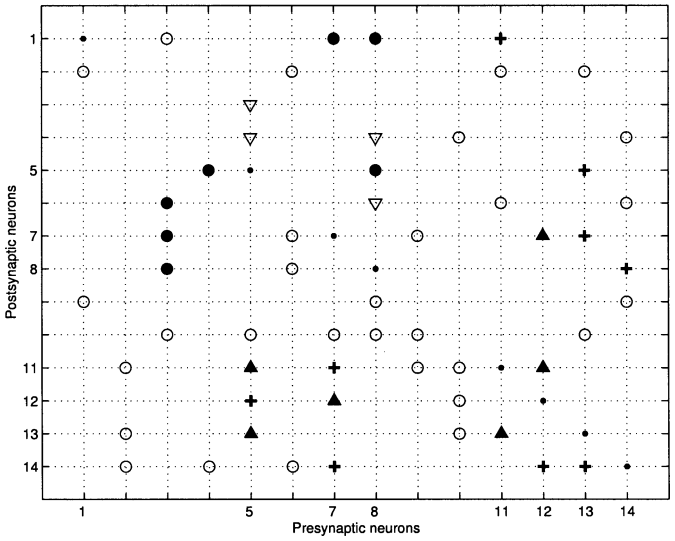
In this paper, we further investigate the plasticity at the network level by showing that the network is able to "store" information about two patterns by means of the appropriate sequence of synaptic potentiations and depressions. By "pattern," we mean here a given distribution of mean firing rates induced by an external stimulation. In order to observe nontrivial rearrangements of subsets of potentiated and depressed synapses, we choose to use the stochastic external signal for stimulating the network, since when too few synapses are simultaneously potentiated, the above noise generation mechanism with deterministic external currents is not sufficient.

Only few synapses are directly observable, so we had to resort to indirect ways to assess the effect of a stimulation of the synaptic efficacies. Specifically, we adopted the following protocol, suited for exposing synaptic changes through changes in the neurons' firing rates.

1) The first stage of the protocol is devoted to setting the initial conditions for the synapses. The neurons are decoupled ($I_{J-} = I_{J+} = 0$) and receive constant external current. The parameters of the analog dynamics of the internal variable $V_{\rm syn}$ are such that all synapses should have $V_{\rm syn} = 0$ V. In other words, the "internal" synaptic dynamics is on (and such that all internal variables should be "down"), but it does not affect the neural dynamics, since the efficacy (postsynaptic current) is zero.



(a)



(b)

Fig. 9. Analysis of the effects of two successive stimulations on the synaptic efficacies. (a) effect of the first stimulation. (b) effect of second stimulation. In each figure, a symbol appears for each existing excitatory-to-excitatory synapse. Numbers labeling the x and y axes in the two figures denote the neurons involved in the two stimulations; the latter are also indicated by black dots along the diagonal. The various symbols code for the different combinations of the observed prestimulation versus poststimulation synaptic states, with reference to the expected ones. Black symbols refer to the potentiated state, while white symbols refer to the depressed state. Triangles indicate those allowed synaptic transitions (of either kind) that in fact occurred. Circles indicate situations in which the synapse should, and did, stay unchanged. The + markers signal missed potentiations.

2) Next the neurons are coupled by setting $I_{J-} = 0$ and $I_{J+} \neq 0$; if all synapses are down, the emission rates of all neurons should stay unchanged. This check ensures that all synaptic efficacies are in in the depressed state at the beginning.
3) With coupled neurons ($I_{J-} = 0$ and $I_{J+} \neq 0$), noisy external currents are injected for 40 s in a chosen subset of eight excitatory neurons, which define the "first pattern" to be "learned."

TABLE I
N_p = Number of potentiated synapses due to stimulation.
N_d = Number of depressed synapses due to stimulation

After the first stimulation	Allowed	Occurred
N_p	16	11
N_d	0	0
Errors	-	0

TABLE II
N_p = Number of potentiated synapses due to stimulation.
N_d = Number of depressed synapses due to stimulation

Second stimulation	Allowed	Occurred
N_p	15	9
N_d	4	4
Errors	-	0

4) We adopt a stimulation protocol specifically devoted to expose the effects of the preceding stimulation on the synaptic efficacies, as explained (in the following, we will refer to this stage as *synaptic check*). The expectation is that the synapses connecting stimulated neurons should make a transition to the potentiated state, while all the others should stay in the prestimulation depressed state. We remark that we do not attempt, in this study, to explore scenarios of very slow learning. However, 40s is a long time compared to the interspike intervals and to a reasonable duration for a single stimulus (with 0.2–0.5 s per presentation, 40 s would correspond to 80–200 repetitions of the same stimulus).
5) After checking the effect of the first stimulation, the network is stimulated with a second pattern, i.e., a different choice of the subset of stimulated neurons. Specifically, again eight excitatory neurons are stimulated, four of which were stimulated also for the first pattern, and four were previously quiescent during stimulation. The expectation is now that the synapses connecting stimulated neurons should stay/become potentiated, for neuron pairs stimulated/not stimulated for the first pattern; previously potentiated synapses which now have a nonstimulated postsynaptic neuron are expected to make a transition to the depressed state.
6) The *synaptic check* is performed again.

The *synaptic check* is performed as follows. After completion of the first stimulation, consider a given neuron and the effect of the stimulation on the synapses on its dendritic tree. Some of these synapses have undergone a potentiation, while some others have been left unaffected and maintain the depressed state. The synaptic dynamics is now frozen by setting $I_{\mathrm{biasn}} = I_{\mathrm{biasp}} = 0$ (zero upward and downward jumps of the internal synaptic variable V_{syn}) such that whatever synaptic efficacies are chosen, the *synaptic check* stage does not affect the synaptic configuration induced by the stimulation. We also set $I_{J-} = 0$ and $I_{J+} \neq 0$. Let us name the spike emission rate of the chosen neuron as ν_{post} and ν_k the one of its kth neuron on its dendritic tree. First, we inject a given current into the chosen neuron (none of the other neurons in the network receive external currents) and measure ν_{post}; next, we inject current in one of the k afferent neurons at a time and measure each time the resulting ν_{post}. The parameters are chosen such that it is highly unlikely for other postsynaptic neurons of neuron k and those of *post*, which do not receive external current, to fire just because neuron k or *post* fired. So an increase in ν_{post} when neuron k is also stimulated signals a potentiated state of the corresponding synapse. Since the depressed state is chosen to have efficacy 0, it is signaled by an unchanged ν_{post}. This procedure for measuring the synaptic states provides an indirect evidence that the second pattern presented to the network is learned and gives strong indications that it would be retrievable in a larger network. Indeed, those postsynaptic neurons which were previously inactive for the first pattern and active for the second pattern will receive a stronger input at the end of the second stimulation. Analogously, synapses on the dendritic trees of those neurons which were active for the first pattern and inactive for the second ones are depressed. The analysis is illustrated in Fig. 9, and some key features are summarized in Tables I and II.

Notice that this protocol is designed to expose in a clear and simple way the synaptic changes induced by the repeated presentations of the second pattern. If the presentations of the second pattern were intermixed within the presentations of the first pattern, then both the two patterns would be learned. Indeed, following each presentation, the synapses to be changed are randomly selected, and those which remain unmodified retain information about previous experiences. A clear indication that this is the case also in our simple protocol is provided by two facts: 1) not all the synapses which are supposed to be potentiated are actually changed, even after such a long stimulation and 2) when the very same protocol is repeated, the synapses which are actually changed differ from trial to trial (not shown in the figure), except for those which are systematically selected, or not, because of inhomogeneities in the synaptic devices, and/or large differences in neural activities in such a small network. These two facts indicate that a stochastic selection is actually implemented in our network and that it would allow for a balanced distribution of memory resources among different patterns in the case of a more natural stimulation protocol and in a larger network.

V. Conclusion

We described a pilot implementation in the relatively unexplored area of analog VLSI *recurrent* networks of spiking neurons, with *on-chip* unsupervised synaptic dynamics.

Many successful developments in the field of neuromorphic engineering dealt with sensors (visual or auditory) and simple networks designed to provide quick and simple decisions on the basis of sensory information, suited for robot guidance in simple environments (see, for example, [14]). Though those efforts have been, and are, invaluable in sharpening techniques and supporting the feasibility and soundness of the neuromorphic approach to "natural computation," there is little doubt that really interesting neuromorphic systems endowed with complex computational abilities will integrate sensors and

"decision modules" with intermediate layers of computation, taking care for example of "classification" of sensory stimuli, which is a necessary function in view of operation in a realistic environment.

Classification tasks have been in the focus of theoretical research in computational neuroscience for long, and there is a wealth of knowledge to be used to derive design principles for "neuromorphic classifiers" (just to mention relevant keywords, the whole *attractor* picture emerging from *Hebbian* learning in networks of spiking neurons with high feedback and providing models of *working memory* states provides an example).

The small network described in the present paper includes the essential elements needed to implement such Hebbian spike-driven plasticity through a stochastic mechanism which selects actual changes in the synaptic efficacies, out of the eligible ones, following the approach briefly outlined in the Introduction; stochasticity is autonomously generated by the network activity, thus providing a key plausibility element.

Scaling up the described architecture poses a number of nontrivial problems. The first is related to the recurrent connectivity of the network: As the number of neurons N increases the number of synaptic connections can grow as much as N^2, and clever packing strategies have to be devised in order to optimize the layout and the routing of the chip, due to both considerations of total silicon area and cross-talk effects.

Besides, the I–O channels needed to experiment with such systems constitute quite a complex complement to the chip. Again, the needed communication bandwidth badly scales with the size of the network (for a given average emission spike rate of each neuron).

We faced the first packing problem in developing a bigger network (128 neurons about 3000 synapses) [15] to be described elsewhere, in which an optimization algorithm has been developed to find the "best" placement and routing of synaptic connections.

As for the communication issues, it has long been suggested that a communication channel suited for connecting neuromorphic devices should exploit the asynchronous, instantaneous, and stereotyped nature of the spikes such as address event representation (AER) bus [16], [17]. Following the AER principles, we developed a communication system based on a programmable interface connecting the AER bus to the standard PCI bus, and a flexible setup is under development, that is suited to deal with several chips implementing large networks [18].

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