# AN ON/OFF TRANSIENT IMAGER WITH EVENT-DRIVEN, ASYNCHRONOUS READ-OUT

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**ABSTRACT**

This paper describes the implementation of a CMOS image sensor that performs a two-way rectified temporal high-pass filtering operation on the incoming visual signal. The sensor adapts to background illuminance and responds to local positive and negative illuminance transients at separately coded terminals. The transients are converted into a stream of asynchronous binary pulses, which are multiplexed onto a common address bus, where the address encodes the location of the sending pixel and the sign of the transient. Gain, response threshold, and refractory period of the pixel output signals can be regulated. The version of the imager described here has an array of 48×48 pixels and was implemented with 0.35 $\mu$m CMOS technology.

## 1. INTRODUCTION

The high density of visual information in our environment makes real-time image transmission and processing a major challenge, in spite of the ever increasing speed of available electronic processing circuits. However, image data tends to be highly redundant and thus compressible without information loss. Furthermore, for a given application, part of the image information may be irrelevant and can be discarded. In order to alleviate the bandwidth requirements of multiplexed data transmission and processing channels, suitable prior reduction and coding of the image data is highly desirable. This can partly be achieved by performing local image processing operations concurrently at each location of visual data acquisition (pixel) in the focal plane. A very basic and useful image compression function is the enhancement or extraction of fast temporal changes in the image. This is particularly true for highly correlated time-variant images with large static regions. The resulting sparse image coding calls for the use of signal multiplexing techniques that are more efficient for such data than the widely-used progressive scanning techniques [1].

As a substrate for electronic imaging and focal-plane image processing CMOS technology has been gaining new interest in the past years as a consequence of its rapid development, which is driven by the computer industry [2]. This leads to continuing miniaturization and improvement coupled with inexpensive fabrication and low power consumption. Due to the essentially two-dimensional structure of CMOS and most other integrated circuit technologies, image acquisition and processing elements have to be interlaced in the focal plane and there is a trade-off between image resolution and parallel processing power. Given the resulting requirement of high processing densities and the analog nature of the optical input signal analog approaches for parallel focal-plane image processing compare favorably with digital solutions for the implementation of various functions.

In this article, we present a focal-plane image sensor and preprocessor with compact pixels that respond to positive (ON) and negative (OFF) illuminance transients at separate terminals. The sensor read-out is event-driven and asynchronously multiplexed on a binary address bus. The read-out interface is fully arbitered and provides four-phase handshaking with a receiver module according to a widely accepted standard [1].

Most previous implementations of optical transient sensors either do not provide rectified ON and OFF output channels [3, 4, 5, 6, 7, 8] or they are significantly larger than the proposed sensing pixel [9, 10]. This pixel is also more compact and less noise-prone than a previously reported circuit using a similar temporal differentiation technique [11].

Implementations of the presented image sensor have already successfully been used as front-ends for a variety of biologically-inspired image-processing circuits that perform such functions as motion-sensing [12], attentional selection [13], and orientation tuning [14].

## 2. PIXEL

The sensor pixel, shown in Fig. 1, consists of two subcircuits. The first subcircuit performs the photosensing and basic signal processing operations. It consists of a photodiode $\mathrm{D}$ in series with a transistor $\mathrm{M_{fb}}$ in source-follower configuration and a negative feedback loop from the source to the gate of $\mathrm{M_{fb}}$ [15]. The feedback loop consists of a high-gain inverting amplifier in common-source configuration ($\mathrm{M_n}$, $\mathrm{M_p}$) [15] and a thresholding and rectifying temporal differentiator stage ($\mathrm{M_{on}}$, $\mathrm{M_{off}}$, C) [11]. The photosensing subcircuit has been analyzed in some detail and will be presented elsewhere [16].

The second subcircuit is responsible for the analog-to-digital signal conversion and for the interfacing with asynchronous read-out circuitry for a two-dimensional pixel array. A mirrored version of each of the rectified signal currents ($I_{on}$, $I_{off}$) of the temporal differentiator is integrated on a capacitor ($\mathrm{C_{on}}$, $\mathrm{C_{off}}$). A tunable, constant leakage current from the capacitor (through $\mathrm{M_{lon}}$, $\mathrm{M_{loff}}$) provides a threshold for the magnitude of the signal current to evoke a response. The voltage ($V_{on}$, $V_{off}$) on the capacitor feeds into a high-gain amplifier, consisting of an activating transistor ($\mathrm{M_{ryon}}$, $\mathrm{M_{ryoff}}$) and a pull-up transistor that is global to each row in the array (not shown in Fig. 1). This amplifier performs a one-bit analog-to-digital conversion and its output pulse $/ry$ initiates a handshaking cycle with a binary row arbiter tree. Once the arbiter has selected a row it sends an acknowledge sig-

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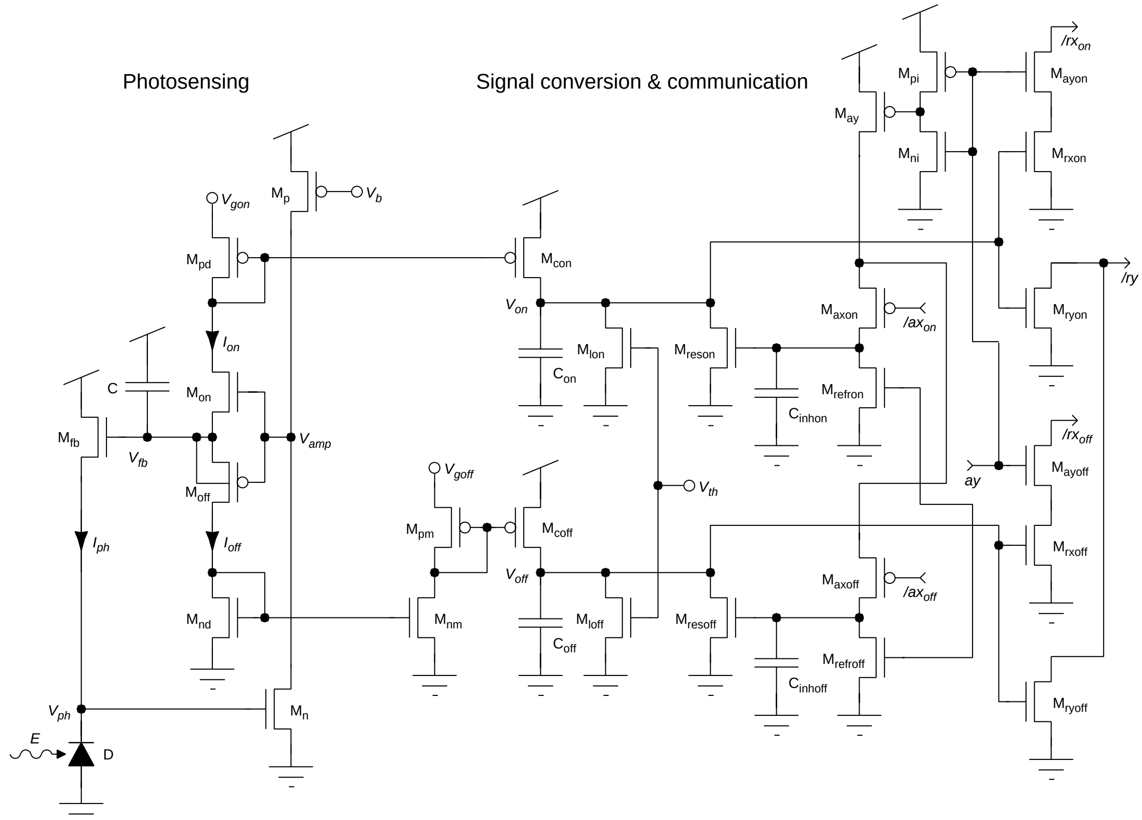



**Fig. 1**. Circuit diagram of the pixel.

nal $ay$ to the pixels in that row. This acknowledge signal enables, via a binary switch ($\mathrm{M_{ayon}}$, $\mathrm{M_{ayoff}}$), a second high-gain amplifier, consisting of an activating transistor ($\mathrm{M_{rxon}}$, $\mathrm{M_{rxoff}}$) and a pull-up transistor, that is global to each column in the array (not shown in Fig. 1). The output signal ($/rx_{on}$, $/rx_{off}$) of this circuit initiates the handshaking cycle with the column arbiter. The column acknowledge signal ($/ax_{on}$, $/ax_{off}$) and the still active row acknowledge charge a capacitor ($\mathrm{C_{inhon}}$, $\mathrm{C_{inhoff}}$) in the selected pixel through a series transistor pair ($\mathrm{M_{ay}}/\mathrm{M_{axon}}$, $\mathrm{M_{ay}}/\mathrm{M_{axoff}}$). The rising voltage on this capacitor opens a transistor ($\mathrm{M_{reson}}$, $\mathrm{M_{resoff}}$), that rapidly discharges the integrating capacitor ($\mathrm{C_{on}}$, $\mathrm{C_{off}}$). Recharging of $\mathrm{C_{on}}$ and $\mathrm{C_{off}}$ is inhibited for a time period that depends on the strength of the input signal and on the discharge rate of the capacitor ($\mathrm{C_{inhon}}$, $\mathrm{C_{inhoff}}$) at the inhibition node, which is set by the current through a leak transistor ($\mathrm{M_{refron}}$, $\mathrm{M_{refroff}}$). The leakage current and therefore the refractory period of each pixel can be globally controlled for the array with a bias voltage.

## 3. IMAGE SENSOR

A 48×48 array of such pixels has been integrated with peripheral arbitration and communication circuitry using standard CMOS technology. A block diagram of the circuit for a reduced-resolution image sensor is shown in Fig. 2.

Each row and each column of the array has a binary address assigned to it, such that each pixel is coded with a unique address. Since each pixel has an ON and an OFF terminal, the terminal type is coded by an additional address bit that it added to the column address. For the 48×48 pixel array a 13-bit address bus is therefore used.

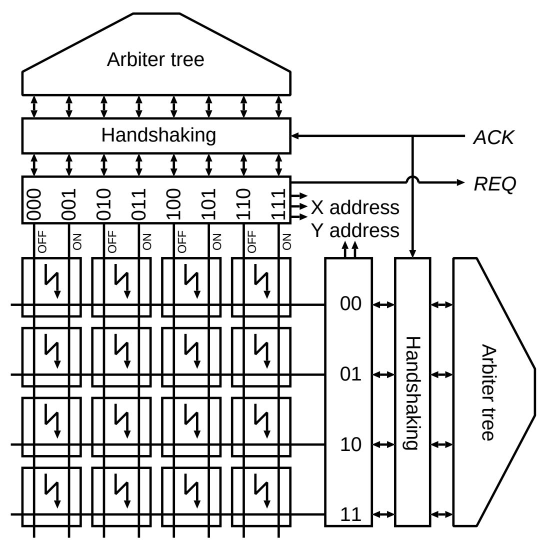
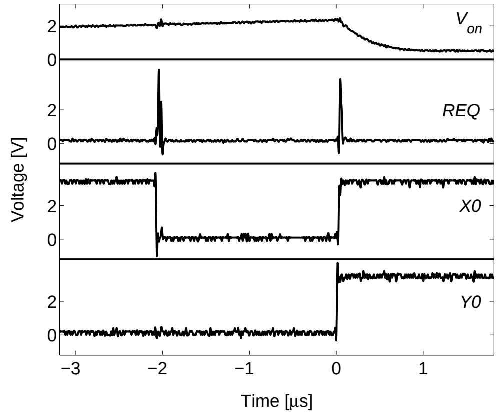
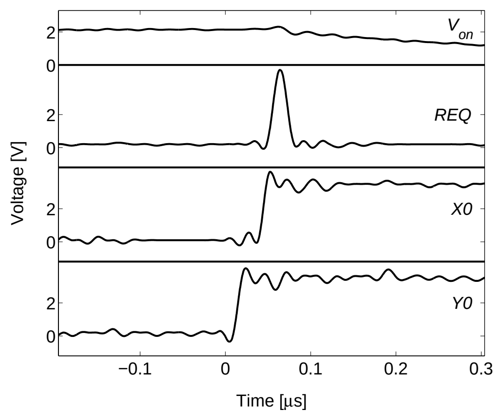



**Fig. 2**. Block diagram of the transient image sensor (reduced resolution).

Arbitration between rows and columns is performed by separate binary arbiter trees. Each arbiter tree receives request signals from the array and returns an acknowledge signal to the selected line after having placed its address onto the bus. If there is more




(a)




(b)

**Fig. 3**. Communication signals in response to a moving dark-to-bright 90% contrast boundary for shorted handshaking terminals on (a) a coarse and (b) a fine time scale. The pixel's transient node voltage $V_{on}$ increases with the accumulated ON transient signal, until it reaches the threshold to activate the communication cycle with the arbiters. After the row arbitration, the row address of the pixel (of which the least significant bit $Y0$ is shown) is placed onto the bus. Subsequently, the column arbitration is performed and the column address (represented by the least significant bit $X0$) is put onto the bus. At the same time, the handshaking request signal, $REQ$ is activated. The acknowledge signal from the arbiter to the pixel resets $V_{on}$. (Note that the observed decay time constant of $V_{on}$ is limited by the read-out instrumentation circuitry, rather than by the actual resetting time. In (a), the previous communication cycle, selecting a different pixel, is also shown.

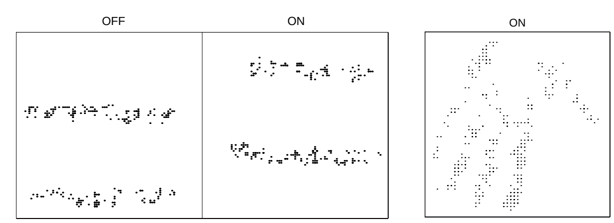
than one request active at the same time the requests are stored in a queue. Row arbitration precedes column arbitration and is blocked, as long as any pixel in the selected row is requesting. The binary structure of each arbiter tree also results in the selection of nearby inputs in consecutive readings, if a multitude of inputs is active. These local preferences provide a speed advantage with respect to first-come-first-serve selection, because of the reduction in arbitration overhead and associated signal propagation delays. The used scheme therefore combines the speed advantage of a progressive scanner with the communication bandwidth reduction of an event-based read-out.

As soon as the complete address of a pixel terminal is available on the bus, a request ($REQ$) handshaking signal is sent off chip that starts the handshaking with an external data-reading device. Once the receiving device has responded with an acknowledge ($ACK$) signal, the next pixel can be selected. A four-phase handshaking scheme is used, where $REQ$ activates $ACK$, which then inactivates $REQ$, which in turn inactivates $ACK$. The arbitration and communication circuitries have been adopted from [1].

If the array is used for imaging purposes under constant or slowly-varying ambient lighting conditions, it only responds to boundaries or edges of moving objects or shadows and not to static scenes. Depending on the settings of the different bias controls the imager can be used in different modes. Separate gain controls for ON and OFF transients allow to make the imager respond to only one type of transient or to both types with adjustable weighting. The threshold bias, together with the gain controls, sets the the contrast response threshold and the rate of spontaneous activity (which can be completely suppressed, if desired). The refractory period control limits the maximum spike rate of each pixel. For short refractory periods, each contrast transient at a given pixel triggers a burst of spikes; for long refractory periods, a typical transient only triggers a single spike in the pixel, resulting in a very efficient, one-bit edge coding.

## 4. EXPERIMENTAL RESULTS

The sensor was tested in an imaging system with a 2.5 mm lens under AC fluorescent office lighting. For the measurements, the $REQ$ and $ACK$ terminals of the chip were shorted, such that the communication speed was only limited by the chip.




(a) (b)

**Fig. 4**. Images recorded by integrating spikes within a 2.5 ms time window. The refractory period was chosen to be larger than the time window, such that each pixel responded at most once, which results in binary images. Spontaneous activity was completely suppressed. (a) OFF and ON response to a stripe stimulus. (b) ON response to a hand.

Figure 3 shows the voltage $V_{on}$ on the integrating capacitor of a pixel, the $REQ$ signal it triggers and the associated transitions in the least significant address bits in response to a moving stripe stimulus. The biases of the multiplexing circuit were set to minimize the communication cycle. The maximum possible data rate for this setting was 20 MHz. The actual pixel read-out rate depends on the relative locations of successively selected pixels. The maxi-

**Table 1**. Characteristics of transient image sensor.

| | |
|---|---|
| Fabrication technology | 0.35 $\mu$m CMOS 2P 4M |
| Resolution | 48×48 |
| Fill factor | 9.2% |
| Pixel size | $(32.8\,\mu\text{m})^2$ |
| Imager size | $(1.68\,\text{mm})^2$ |
| Die size | 2.29 mm×2.12 mm |
| Operating range | 1.5 lx–3000 lx (66 dB) |
| Max. pixel read-out rate | 20 MHz |
| Max. full-frame read-out rate | 3 kHz |
| Power supply voltage | single 3.3 V |
| Power dissipation (at 20 lx)<br>Quiescent<br>Max. activity (20 MHz) | <br>2.25 mW<br>55.85 mW |
| Max. read-out conversion gain | $2.82\times10^{-6}$ events/$e^-$ |
| Saturation level<br>Single-pixel activation<br>Full-field activation | <br>$7.08\times10^{12}$ $e^-$/s (1.13 $\mu$A)<br>$1.54\times10^{9}$ $e^-$/s (247 pA) |

mum full-frame read-out rate was determined to be 3 kHz when the entire array was illuminated with a square-wave modulated LED. The power dissipation strongly depends on the data rate, ranging from 2.25 mW in the absence of any activity to 55.85 mW for the maximum data rate at a background illuminance of 20 lx. If the imager is used in conjunction with a receiving device, matching of the communication cycles of sender and receiver minimizes power dissipation and arbitration queues.

The response of the sensor to different stimuli is shown Figure 4. The images were obtained by mapping out the addresses read from the image sensor within a given time window. A long refractory period was used, such that no pixel responded more than once and the images are therefore binary.

The characteristics of the imager are summarized in Table 1.

## 5. CONCLUSION

An image sensor that encodes the contrast of illuminance transients, rather than raw illuminance has been presented and characterized. ON and OFF transient responses are encoded separately and can thus be individually controlled. The DC response is small and can be completely cancelled, which results in efficient signal coding, noise suppression, and low DC power consumption. The sparse signal representation together with a standardized, event-based multiplexing strategy allow for high-speed data communication and facilitate image processing by successive circuits. The sensor has been successfully interfaced to a variety of image processing modules, that use the same asynchronous communication standard.

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