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A novel ADPLL design using successive approximation frequency control

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ABSTRACT

This paper presents a hardware implementation of a fully synthesizable, technology-independent clock generator. The design is based on an ADPLL architecture described in VHDL and characterized by a digital controlled oscillator with high frequency resolution and low jitter. Frequency control is done by using a robust regulation algorithm to allow a defined lock-in time of at most eight reference cycles. ASICs in CMOS AMS 0.35 μm and UMC 0.13 μm have been manufactured and tested. Measurements show competitive results to state-of-the-art mixed-signal implementations.

1. Introduction

The fast creation of complex system on chip (SoC) designs consisting of several intellectual property (IP) cores is state of the art for standard digital functionality [1]. A problem in this context are mixed-signal subblocks within the chip. These are highly technology dependent and a time-consuming re-design is necessary when technology or application area are modified [2].

An essential part of most modern digital circuits is a clock generator. This could be used to generate a high working frequency out of a much lower reference. It is also possible to regulate this output frequency dynamically with regards to low power design. The usage of a phase locked loop (PLL) architecture is a very effective way to form this function block. A PLL tries to synchronize a reference frequency with the output frequency of an oscillator by adjusting the latter.

Classical PLL implementations rely on analog components [1]. Because of this they are not suited for usage as an IP core. As mentioned above an extensive re-design has to be done any time the technology or the frequency specification is changed. A new approach is all-digital PLLs (ADPLL). Their hardware implementation consists completely of digital standard cells [1,2]. The phase detector, loop filter and frequency divider can easily be described in a high level hardware description language (HDL) to form a technology-independent softcore [1–3]. More difficult to implement is the digital controlled oscillator (DCO). The DCO designs presented in [1,4] still require a time-consuming manual fine tuning depending on the target library to meet the specified frequency and jitter specification. Compared to that, the clock generator design presented in this paper could be implemented in the same fast and easy way as a typical IP core in every standard digital synthesis-based design flow. This is realized by a combination of the standard-cell-based low jitter DCO presented in [3,5] and a robust frequency regulation algorithm based on successive approximation, as described in the following.

2. ADPLL concept description

The main application of such an ADPLL will be in supplying a clock reference for distributed digital processing systems on an SoC, based on one master reference clock. This design target necessitates a very high accuracy with respect to the master clock.

2.1. Architecture

The ADPLL is based on an architecture documented in a recent patent [5]. Long-term frequency stability and fine tuning of the output signal is achieved via switching between two adjacent lengths using a fractional divider (here called modulo *M* unit). Analytical jitter descriptions of this architecture have been derived in Ref. [3].

Since the clock is intended for digital processing systems, no analog fine tuning of the DCO delay elements is required. Besides long-term accuracy, the only additional requirement is that the jitter is small enough with respect to the clock period not to violate timing constraints of digital circuits supplied by this clock. This can be assured by using fast single elements in the DCO chain, where switching between two adjacent lengths does not substantially alter the basic clock period (Fig. 1).

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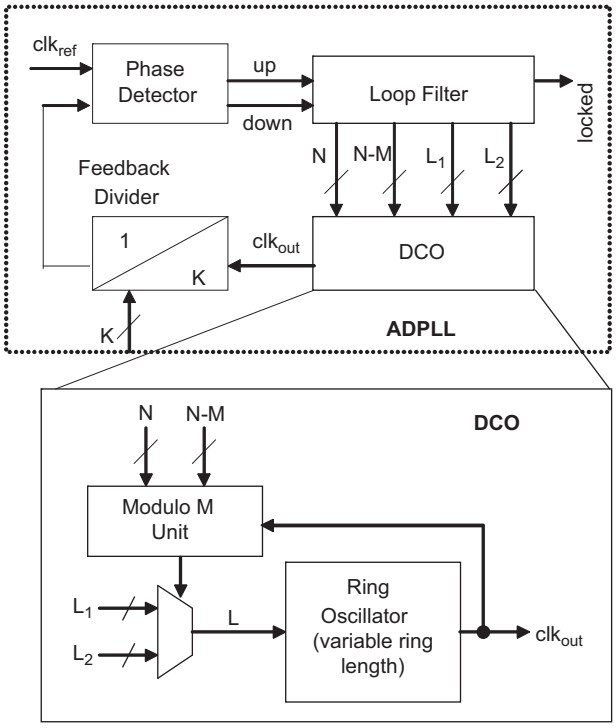

Fig. 1. Architecture of the discussed ADPLL.

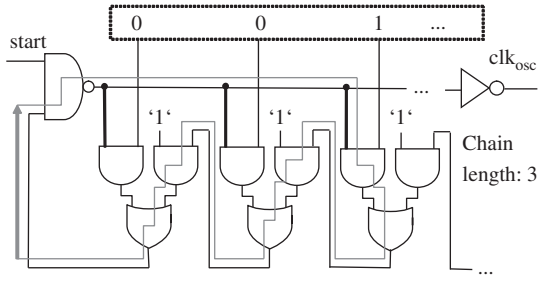

Fig. 2. Oscillator chain for a one-hot coded length of three.

As shown in Fig. 2, the DCO chain consists of AND–OR combinations which can be easily set to a defined chain length via a one-hot coded configuration word and have low propagation delay [3,6], in our case typically 80 ps for an AND–OR in 0.13 μm, respectively, 290 ps in 0.35 μm. When taking into account a factor of 2 for a full clock cycle (i.e. a high–low and a low–high transition), this compares well with the measured delays as shown in Figs. 17 and 18.

The basic building blocks as detailed above are the same for both presented implementations of the PLL. Compared to the 0.35 μm PLL, the 0.13 μm PLL has been designed for a higher clock reference, so the maximum multiplication factor of the feedback divider has been reduced. Additionally, the 0.13 μm PLL features a programmable output frequency divider that can be programmed independent from the feedback divider, thus allowing a wider frequency range of the output clock.

2.2. Functional description

In extension of the patented features [5], the architecture presented here is characterized by a technology independent, successive approximation type DCO frequency acquisition, with coarse tuning of the ring length and subsequent fine tuning of the fractional divider ratio (see Fig. 3).

Usually, the target frequency will correspond to an intermediate chain length between two discrete lengths L1 and L2. Once this chain interval has been found according to the procedure in Fig. 3, a similar successive approximation is used to find the ratio N/M of the modulo M unit (see Fig. 4).

If the regulation is down to switching the last bit of N, the PLL has achieved a lock on the frequency. The DCO is adjusted with both rising and falling edges of the reference clock, resulting in a lock acquisition of less than eight reference cycles. Once the fine trim is achieved, two adjacent chain lengths L1 and L2 have been selected, which are closest to the target frequency. The appropriate ratio of the usage of those chain length by the ring oscillator to ensure overall accuracy of the output frequency is determined by the modulo M unit.

The modulo M unit is central to the idea of long-term accuracy of the PLL output with respect to the reference clock. Since it governs the fine tuning of the output clock frequency and its working is entirely digital and thus free of error, relative clock accuracy can be extended arbitrarily by increasing the counter length of the modulo M unit. The only penalty of this extension is the increased lock time of the fine trim as shown in Fig. 4.

As denoted by the continued switching of the last bit of N in Fig. 4, the frequency regulation is continually active, ensuring a fast lock re-acquisition if the lock on a target frequency is lost (e.g. through temperature variations which may affect DCO delay times). The concept for this lock re-acquisition on the target frequency is a stepwise re-adjustment of both the fine trim and

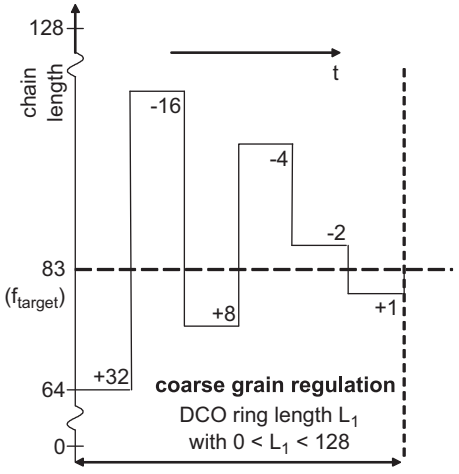

Fig. 3. Frequency acquisition and control scheme of the ring length tuning.

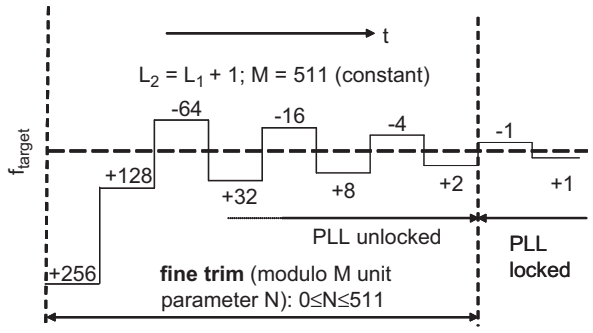

Fig. 4. Frequency acquisition and control scheme of DCO.

the coarse regulation. If the locked modulo M ratio does not correspond to f_{target}, e.g. because of temperature drift, the ratio N/M is adjusted in steps of -1 or $+1$, respectively. If the lower or higher limit of the modulo M unit is reached, the coarse regulation adjusts the ring length by one element. For this new ring length, the modulo M unit is again initialized with its highest or lowest value. This means that frequency readjustment is done in single steps of the modulo M unit even across adjacent ring lengths.

3. Jitter considerations

3.1. Jitter terminology and definitions

Based on the widely accepted definition of jitter [7] as the temporal displacement between ideal and real signals the following quantities are used in further PLL characterization. $T(n)$ expresses the length of the nth period and $T_0 = 1/f_0$ represents the ideal period, respectively, whereby we assume T_0 to be equal to the long-term average of $T(n)$:

$$T_0 = \lim_{N\to\infty}\left(\frac{1}{N}\sum_{n=1}^{N} T(n)\right). \tag{1}$$

The jittering period is described by the rms-value

$$J_{\text{rms}} = \frac{1}{N}\sum_{n=1}^{N} J(n)^2 \tag{2}$$

of the actual period deviation $J(n) = T(n) - T_0$.

Another quantity that helps to gain insight into PLL-operation and correspondent jitter sources is called *TIE* (time interval error) and defined as

$$TIE(n) = t(n) - t_0(n) = \sum_{v=1}^{n} J(v). \tag{3}$$

It should be mentioned that the *TIE* in literature is also referred to as 'timing deviation', 'absolute jitter' or 'cumulative jitter' [8]. Because of the integrating nature of this parameter, temporal dislocations in the long term can be made visible.

In order to compare this digital design to analog counterparts, the commonly used single sided phase noise characteristic [9] has to be derived:

$$\mathscr{L}(\Delta f) = \frac{S_{\text{SS}}(f)}{P_0 \cdot 1\,\text{Hz}}. \tag{4}$$

$S_{\text{SS}}(f)$ is the power spectral density (PSD) with respect to positive frequencies only and P_0 denotes the total power related to the fundamental frequency (here f_0) and is calculated as

$$P_0 = \int_{f=0.5f_0}^{1.5f_0} S_{\text{SS}}(f)\,\mathrm{d}f. \tag{5}$$

Starting with the output waveform $v(t)$ sampled at 4 GS/s, one obtains $v(n) = v(t = n \cdot T_s)$, $n = \{0, 1, \ldots, N\}$ with T_s as the sample period.

Considering Parseval's Theorem applied onto discrete finite sample sequences [10], the single-sided PSD with a sampled sequence as input parameter yields

$$S_{\text{SS}}(f) = \frac{2}{N} \cdot |FFT(v(n))|^2 \tag{6}$$

which represents a spectrum consisting of a set of dirac pulses at $f \in \{0, 1/N \cdot T_S, 2/N \cdot T_S, \ldots, N/2/N \cdot T_S\}$.

For direct comparison with otherwise obtained phase noise characteristics the $S_{\text{SS}}(f)$ should be continuous. Therefore we interpolate between the discrete frequency components. Assuming a constant spectral power density in the interval between those frequencies we obtain

$$S_{\text{SS}}(f) = \frac{2}{N^2 \cdot T_S} \cdot \left|FFT\left(v\left[\text{floor}\left(\frac{f}{N \cdot T_s}\right)\right]\right)\right|^2 \tag{7}$$

$$\text{valid for } f \in \left[0, \frac{1}{2 \cdot N \cdot T_S}\right]. \tag{8}$$

This formula was used to calculate the phase noise curves shown in Section 4.1.

3.2. Influence of the frequency divider

Since one of the designs contains a programmable integer frequency divider at the PLL-output, its influence on jitter and phase noise was investigated. If we derive the by-D-divided period from the sum of uncorrelated $T(n)$

$$T_{\text{div}}(n) = \sum_{D} T(v), \tag{9}$$

it is obvious, that with

$$E(T) = T_0, \quad S(T) = \sigma \tag{10}$$

we obtain

$$E(T_{\text{div}}) = D \cdot T_0, \quad S(T_{\text{div}}) = \sqrt{D \cdot S(T)^2} = \sqrt{D} \cdot \sigma. \tag{11}$$

Simulations were carried out and showed this expected behaviour of the output divider in Fig. 5.

If the single periods $T(n)$ are no longer uncorrelated by means of the principle of this PLL, the overall behaviour of the system is different. The period of the divided clock is now described by

$$T_{\text{div}}(n) = A \cdot T_r + B \cdot T_{r+1}. \tag{12}$$

The factors A and B are determined by the actual N-by-M ratio of the fractional divider and obey $A + B = D$. T_r and T_{r+1} are the resulting periods of two successive lengths of the delay chain. The relative frequency of A and B can be calculated according to the functional principle of this PLL by

$$R_A = \frac{N}{M}, \quad R_B = 1 - \frac{N}{M}. \tag{13}$$

Thus we write

$$E(T_{\text{div}}) = E(A \cdot T_r + B \cdot T_{r+1}), \tag{14}$$

$$E(T_{\text{div}}) = D \cdot \frac{N}{M} \cdot T_r + D \cdot \left(1 - \frac{N}{M}\right) \cdot T_{r+1}. \tag{15}$$

Since T_r and T_{r+1} are meant to be related as $T_{r+1} = T_r + \tau$ we have proven the underlying concept

$$E(T_{\text{div}}) = D \cdot \left(T_{r+1} - \frac{N}{M} \cdot \tau\right) \tag{16}$$

$$= D \cdot \left(T_r + \frac{M - N}{M} \cdot \tau\right). \tag{17}$$

To estimate the standard deviation, following approach is used: the output divider in a switched chain length configuration with a fixed M (511) allows only two discrete values (short and long) for the actual output period, namely

$$T_s = D \cdot T_r - \text{floor}\left(\frac{M}{N \cdot D}\right) \cdot \tau, \tag{18}$$

$$T_l = D \cdot T_r - \text{ceil}\left(\frac{M}{N \cdot D}\right) \cdot \tau. \tag{19}$$

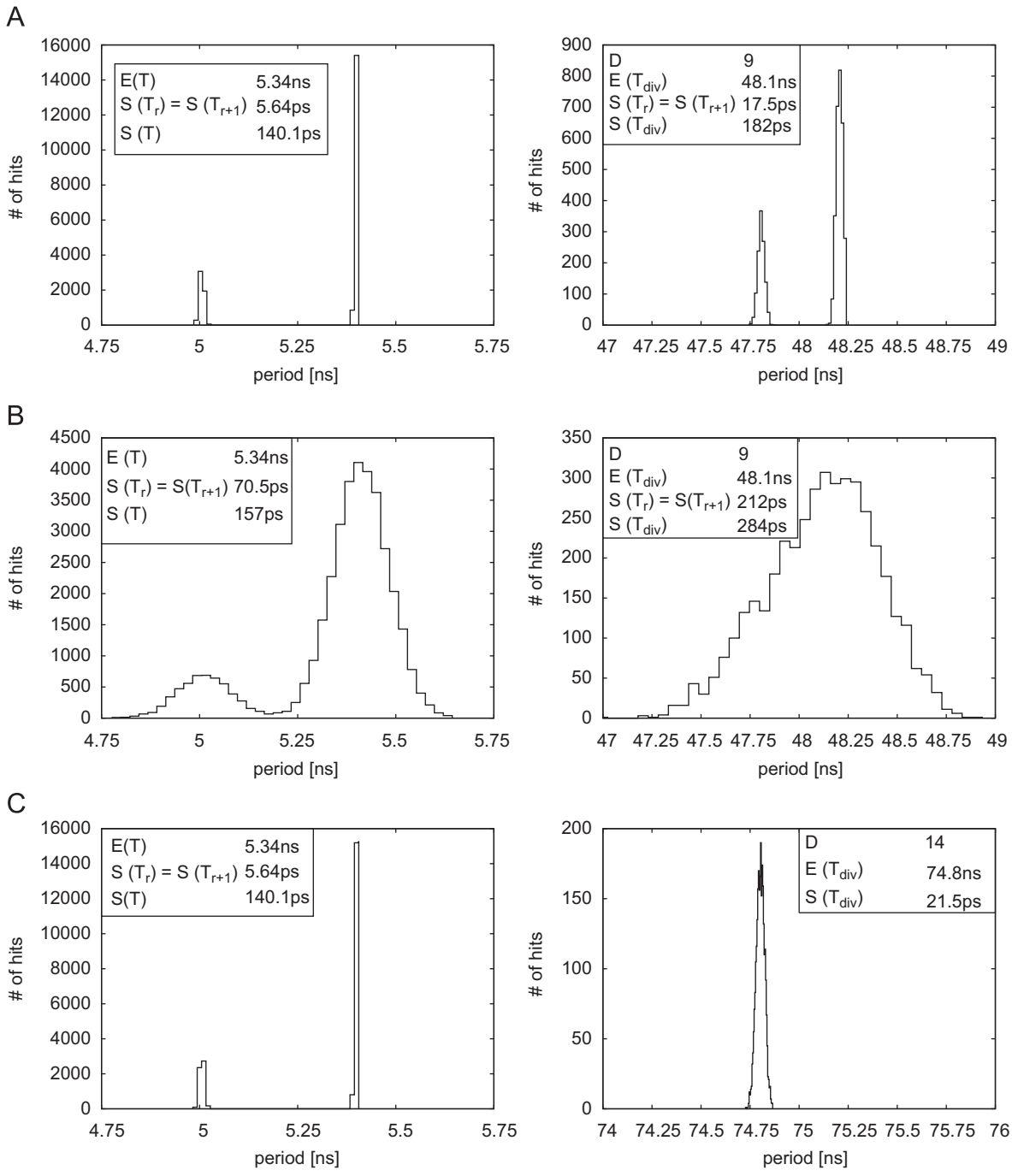

Fig. 5. Simulation with divider $N : M = 73 : 511$. Histogram of periods for undivided (left) and divided (right) clock. (A) $D = 9$, (B) $D = 9$, with additional noise on the output clock of the DLL, (C) $D = 14$.

The relative frequencies of T_s and T_l which determine the final Jitter J_{rms}, can then be described by

$$R_l = \frac{D \bmod \left(\frac{M}{N}\right)}{\frac{M}{N}} \cdot \tau, \tag{20}$$

$$R_s = 1 - R_l. \tag{21}$$

Hence, a masking effect is obvious, because for a certain relation of $M/N \cdot D$ the floor and ceil functions yield the same value and the modulo result is zero. Then the generated output period is a fixed value with the jitter:

$$S(T_{\text{div}}) = J_{\text{rms}} \tag{22}$$

$$= \sqrt{D} \cdot S(T_r) = \sqrt{D} \cdot \sigma. \tag{23}$$

This masking can also be observed, when the modulo is close to zero, since one of the relative frequencies will tend towards zero, thus having only negligible impact on J_{rms}. In general, J_{rms} is determined by

$$J_{\text{rms}} = \int_{-\infty}^{+\infty} R_s \cdot (T_s + N_s(T) - E(T_{\text{div}}))^2 \tag{24}$$

$$+ R_l \cdot (T_l + N_l(T) - E(T_{\text{div}}))^2 \mathrm{d}T. \tag{25}$$

As observed in measurements, a Gaussian distribution is assumed for the noise of each of the two occurring divided periods which are separated by τ. Thus, $S(T_{l,s}) = \sqrt{D} \cdot \sigma$ and the integral J_{rms} cannot be resolved in a closed form.

If the standard deviation of a fixed chain length (σ) is small compared to τ then the final jitter value is predicted by

$$J_{\text{rms}} = R_s \cdot (T_s - E(T_{\text{div}}))^2 \quad (26)$$

$$+ R_l \cdot (T_l - E(T_{\text{div}}))^2. \quad (27)$$

However, if τ is small compared to σ, the jitter is equal to $J_{\text{rms}} = \sqrt{D} \cdot S(T) = \sqrt{D} \cdot \sigma$. This allows for the following conclusion: the rms-jitter after an ideal (non-jittering) output divider in a switched chain length configuration can neither be smaller than the jitter of a fixed chain length signal multiplied by $\sqrt{D}$ nor smaller than the influence introduced by the two occurring discrete periods (T_s, T_l). Those derivations have been verified by system simulations of the proposed oscillator.

When estimating the influence on the value of *TIE*, one simple fact has to be considered. Since the *TIE* is the total sum of all occurred period deviations, the *TIE* of a divided signal cannot differ from the *TIE* of the signal source. The division process can be considered as calculating partial sums, which when summing up themselves yield the same value as summing all periods at once. Fig. 5 validates previously derived formulae and illustrates the effects that come along with switching oscillator chains and frequency division.

4. Measurement data

4.1. Spectral performance

PLL performance is often judged with respect to the spectral components within the clock jitter, especially if this PLL is meant for radio frequency (RF) applications [11]. Since our PLL has been optimized along different targets (i.e. high accuracy digital systems clock), its spectral performance is not sufficient for RF designs.

The underlying PLL principle can be visualized by plotting histograms of the clock periods. Since the PLL fabricated in the 0.13 μm technology is equipped with an additional output divider, its impact for different ratios is also plotted in Fig. 6. Note that for the undivided output of the PLL in Fig. 6 (left), the $N : M$ ratio can be extracted from the period distribution as $473 : 511$. For the divider ratios 4 and 8, the period distribution cannot be as clearly separated and might be different from the one extracted above for divider ratio 1, since the PLL continually adjusts itself. However, since the measurement data in Fig. 6 was taken during the same measurement run (i.e. with limited clock and temperature drift), the $N : M$ ratio should be very similar.

Fig. 7 depicts the calculated phase noise characteristics of a commercial HP33120 (at 15 MHz) oscillator together with the output of the 0.13 μm PLL running at 86 MHz and ratios of 1 and 8. It can be seen that the number of spurs impacting from the 1 MHz reference clock is significantly reduced by the divider, but the phase noise is still much higher than the generator itself.

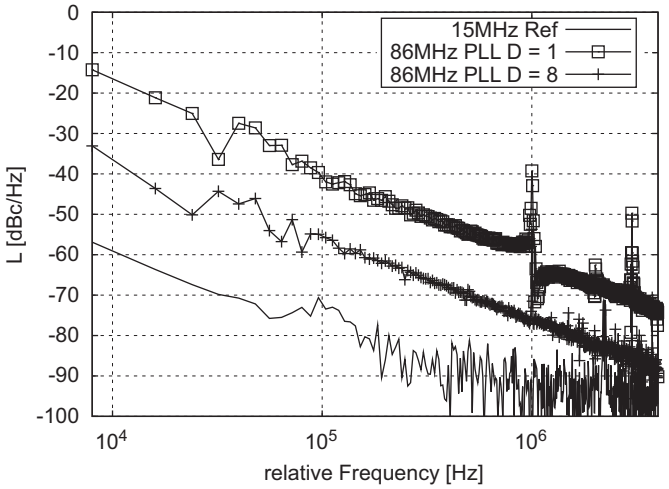

Fig. 7. Phase noise of the 0.13 μm PLL and the reference oscillator.

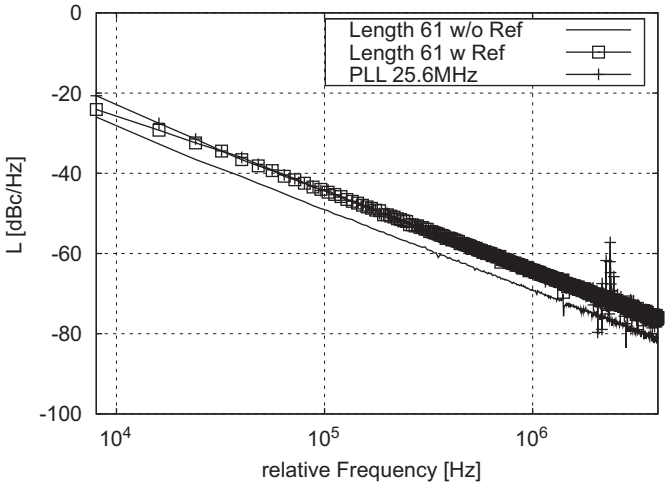

Fig. 8. Phase noise of the 0.35 μm PLL.

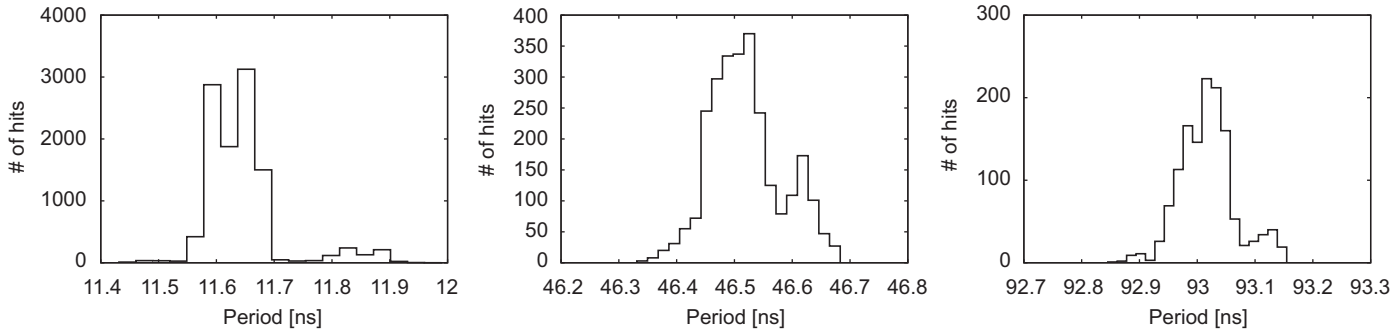

Fig. 6. Measured period histograms of the 0.13 μm PLL at 86 MHz (reference clock 1 MHz, multiplier 86, for $N : M$ ratio see text). The output divider ratio is equal to 1 (left), 4 (middle) and 8 (right), respectively.

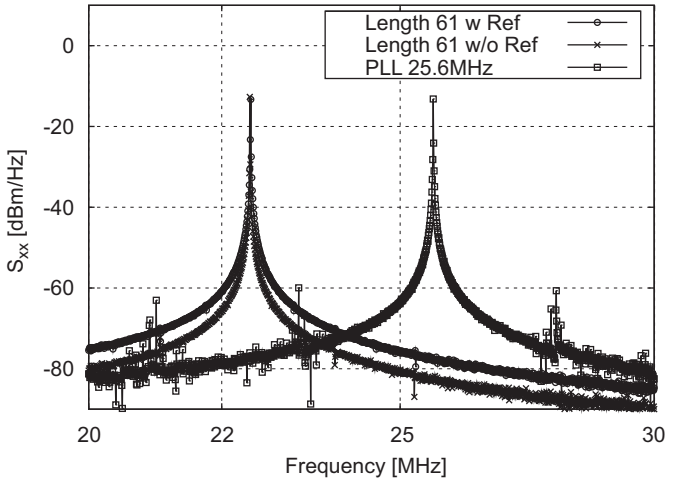

Fig. 9. Output spectrum of the 0.35 μm PLL compared to fixed chain length ring oscillator.

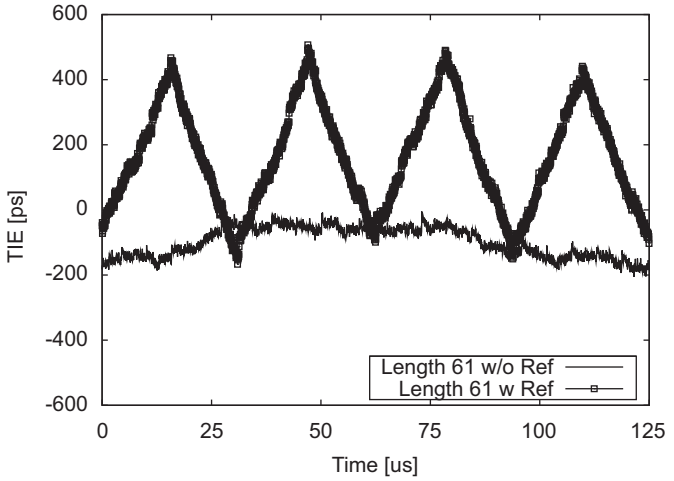

Fig. 10. Timing interval error of 0.35 μm fixed chain length oscillator at $f_{ref} = 32$ kHz.

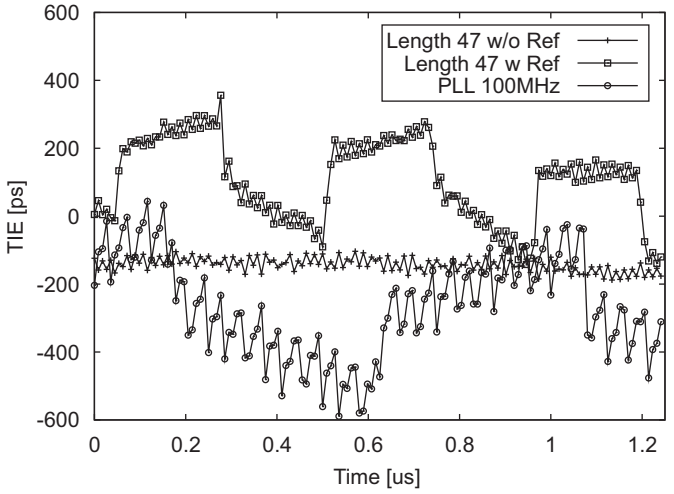

Fig. 11. Timing interval error of 0.13 μm fixed chain length oscillator and PLL at f_{ref} equal to 1 and 2 MHz.

The phase noise of the ADPLL is very high compared to mixed-signal designs [11]. One reason is the usage of fast standard-cell digital gates in the DCO chain, which have a high jitter compared to their mean delay times even for a fixed chain length. When the DCO is used in PLL mode, additional jitter is introduced through the switching, especially around the reference frequency. This is due to the modulo *M* unit operating at the reference clock.

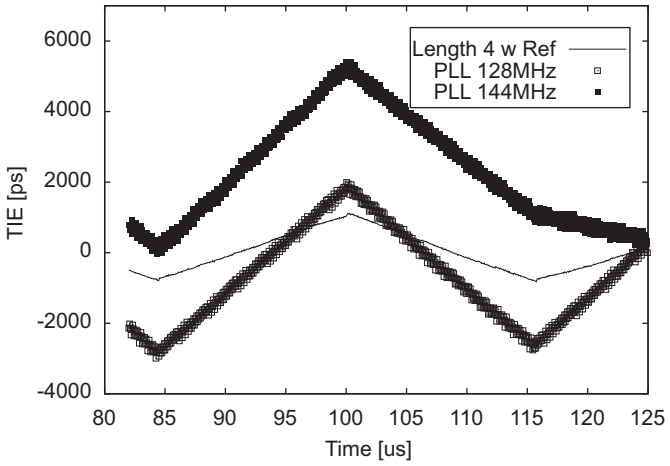

Fig. 12. Illustration of the 0.35 μm PLL influence on *TIE*.

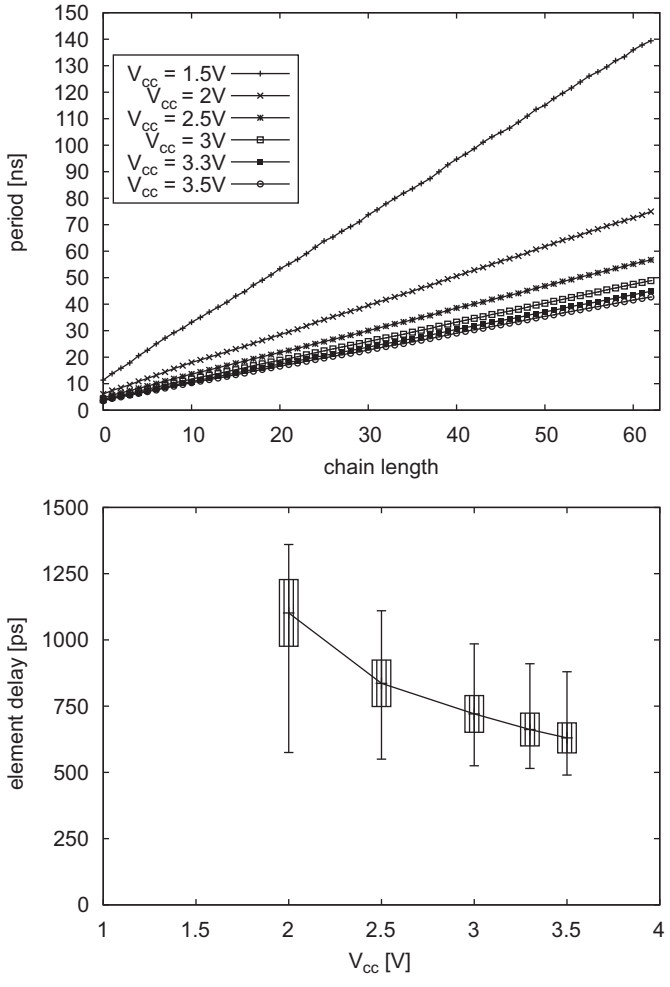

Fig. 13. Period vs. chain length and element delay vs. voltage for the 0.35 μm PLL.

The spectral behaviour could possibly also be derived analytically. For example, Salomon et al. [12] employ calculations similar to Section 3 to estimate the positions and intensities of spurs as related to the switching of transitions in their DDPS-system, which is also characterized by a distribution of discrete period times.

The influence coming from the PLL principle itself can be observed in Fig. 9. Phase noise and output spectrum of the 0.35 µm PLL running at 25.6 MHz are plotted together with the characteristics of the fixed length (chain length = 61) ring oscillator in Fig. 8 (Fig. 9).

The fixed length ring oscillator without applied reference clock shows the purest spectral behaviour.

4.2. Timing and jitter behaviour

The spectral impurities are also reflected in a non-ideal timing interval curve. This is visualized best by plotting *TIE* vs. time (see Fig. 10).

The triangular upwards and downwards movement follows exactly the frequency of the reference clock and can be observed for every setting of chain length, but the impact is the higher the shorter the delay chain. This disadvantageous behaviour is an analogue effect that increases and decreases the delay time of the delay elements, with respect to the current state of the reference clock line. A slightly different impact of the reference clock could be measured in the 0.13 µm PLL, since here additionally the period at a state transition of the reference clock line is disturbed significantly (Fig. 11).

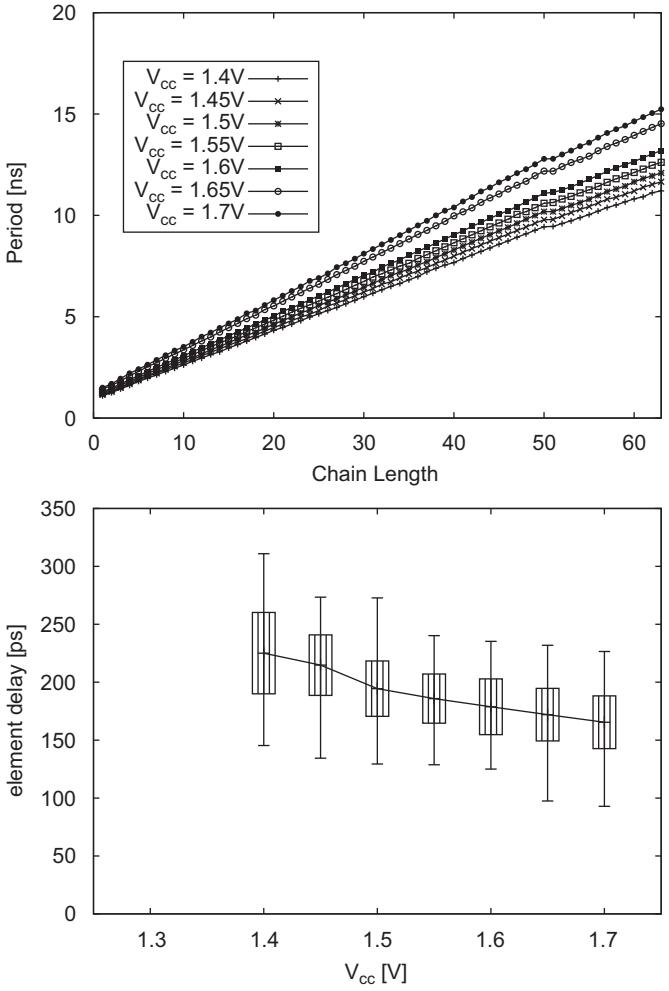

Fig. 14. Period vs. chain length and element delay vs. voltage for the 0.13 µm PLL.

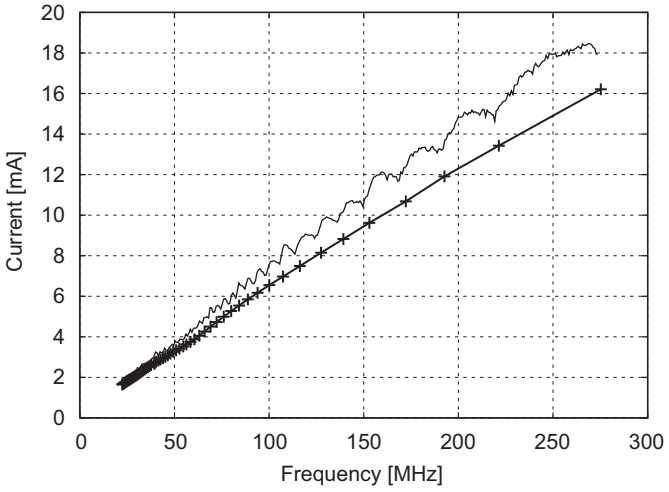

Fig. 15. Current consumption as function of frequency for 0.35 µm PLL.

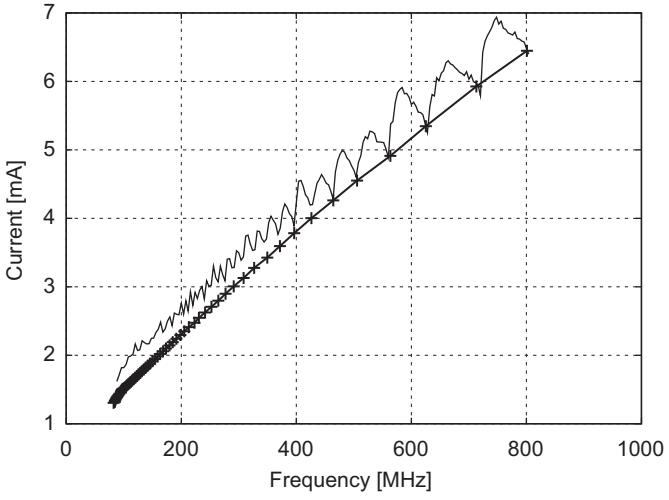

Fig. 16. Current consumption as function of frequency for 0.13 µm PLL.

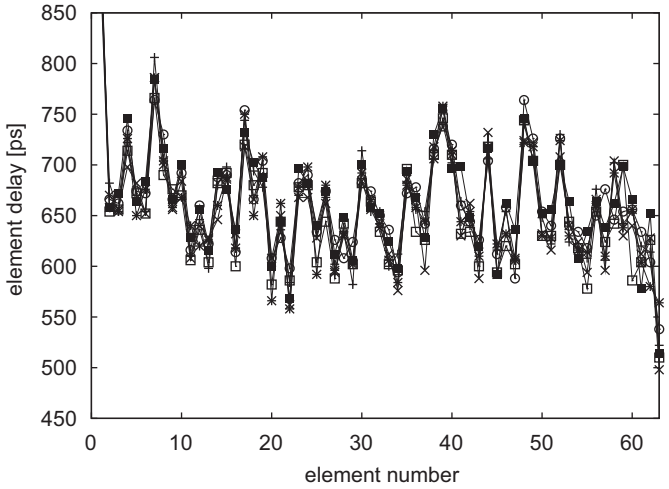

Fig. 17. Delay of DCO elements in chain, measurement curves for several 0.35 µm ICs overlaid.

When in PLL mode the very same effect occurs, but since a switching of clock periods happens all the time, it partially can be regulated out by the control logic. Fig. 12 shows the behaviour in the case of $f_{ref} = 32$ kHz and $f_{PLL} = 128$ and 144 MHz, respectively.

For comparison the pure influence in a fixed chain length configuration (length = 4) is shown. Since the PLL is built to regulate one set of parameters (chain length and fractional ratio) that determine the frequency, the control logic tries to align the output frequency to the reference clock. If in this case the output frequency slightly changes resulting in a continuous 'run-away' from the non-disturbed clock corresponding to the actual state of the reference clock, it cannot find a stable parameter set and thus has to vary the fractional ratio at every edge of the reference clock. This can be seen in the behaviour of the 128 MHz clock, where the ratio varies from $N : M = 210 : 511$ to $211 : 511$ at every reference clock transition. The same happens in the 144 MHz signal, where the ratios are $164 : 511$ and $165 : 511$, respectively. At 115 μs the control logic detects that the reference edge is still within range and therefore skips altering the fractional ratio. The still visible kink at this time is due to the reference impact itself and the difference of the slopes before and after 115 μs are the same as for the free running ring oscillator.

To reduce this effect, the DCO should be adjusted at either the rising or falling edge of the reference clock, but not at both of them.

4.3. Voltage dependency

The voltage-dependent delay characteristic of the delay chain is presented in Figs. 13 and 14. In both oscillators the effect of scaling the supply voltage is very similar. An increased supply voltage leads towards a smaller element delay as has been

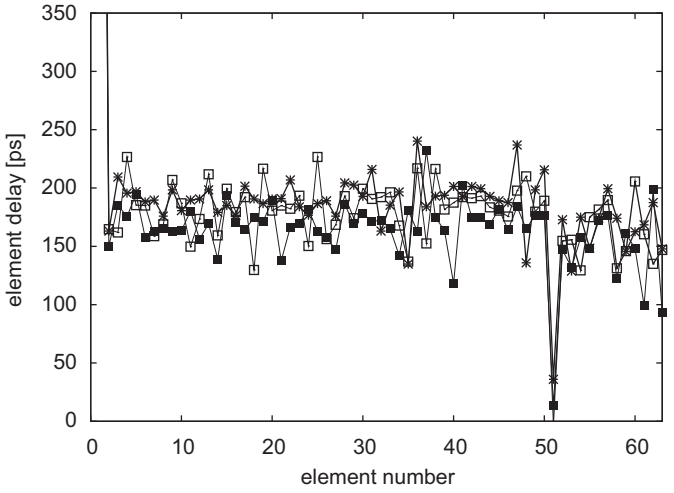

Fig. 18. Delay of DCO elements in chain, measurement curves for several 0.13 μm ICs overlaid.

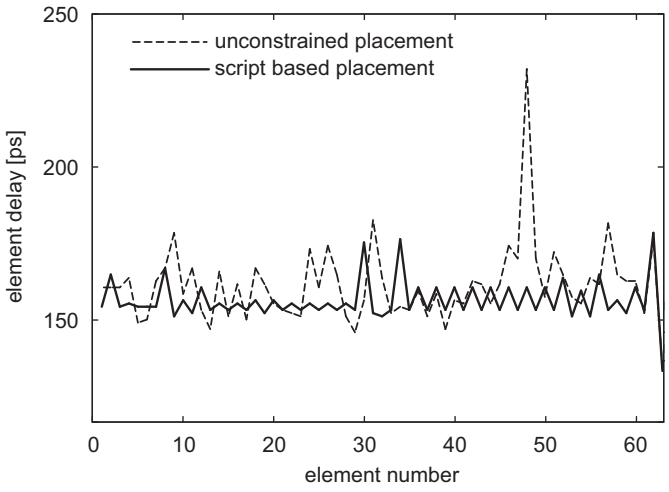

Fig. 20. Simulated delays for regular and irregular placement in UMC 0.13.

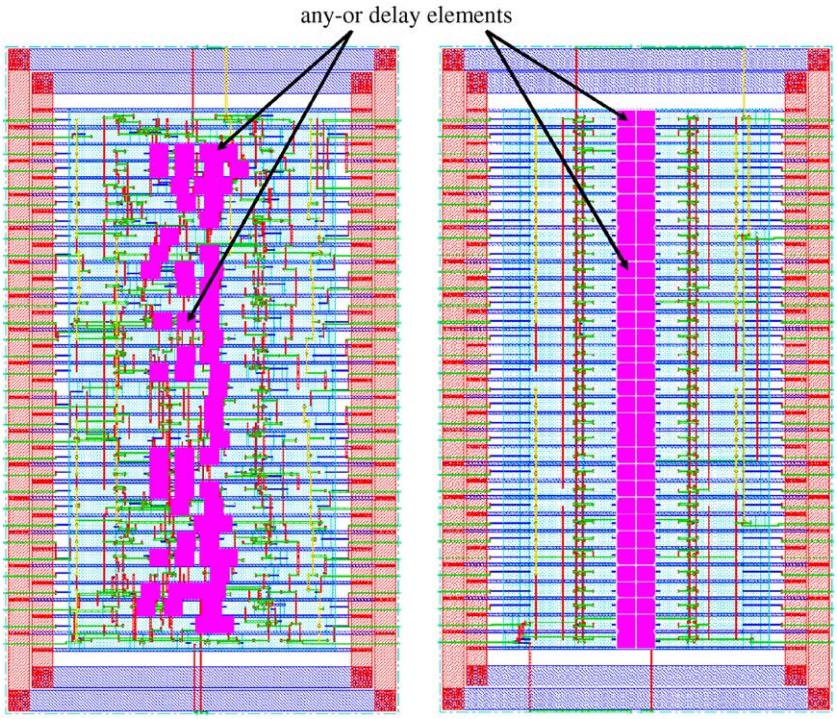

Fig. 19. Irregular and regular placement of the delay elements.

described in the power-law-model by Sakurai [13]. Furthermore the variations of that delay and thus the evenness of τ decreases with voltage as well. But the general PLL operation does not depend on a certain voltage range, since it is only limited by the same voltage boundaries as the application circuitry, that is driven by the generated clock, itself.

4.4. Power consumption

Due to the fact that this PLL is basically a CMOS circuit, its power draw increases nearly linearly as a first order approximation. This holds especially, when the regulation is disabled, since then the only switching occurs in a fixed length ring oscillator. As soon as the regulation loop is closed and the locking process has started some more switching can be observed in the power consumption curve due to the functional principle of this PLL. If the target frequency is directly between two ring delays, the switching frequency of the fractional divider is highest, resulting in the local maxima of the power draw, when compared to the fixed chain length oscillator mode.

The effect of switching between two adjacent ring length for intermediate frequencies can be observed from the 'jittery' curve in Figs. 15 and 16. Compared to the patented version, the fine tuning is done at the reference frequency, which drastically reduces the power dissipation. As can be seen from those figures, the power requirements of the fractional divider are small compared to the linear scaling of DCO ring current with ring frequency. The total power draw of the circuits can be estimated as follows:

$$P_{\mathrm{tot},35} = 1.32\,\mathrm{mW} + 145\,\frac{\mu\mathrm{W}}{\mathrm{MHz}}, \tag{28}$$

$$P_{\mathrm{tot},13} = 1.9\,\mathrm{mW} + 11\,\frac{\mu\mathrm{W}}{\mathrm{MHz}}. \tag{29}$$

The scaling effect of digital power draw for shrinking technology sizes is evident from the above equations. The 0.13 μm PLL has less than one-tenth the frequency-dependent power requirements of the 0.35 μm PLL.

4.5. Aspects of automated digital PLL design

The matching between different sample ICs of the 0.35 μm PLL implementation in Figs. 17 and 18 show that a large proportion of the jitter is due to the haphazard placement of the DCO elements rather than process variations. By using additional constraints to regularize placement and balance wire length within the place-and-route routine, the jitter due to delay variations between consecutive DCO delay gates can be substantially reduced.

To estimate the jitter effect of the automated place and routed delay cells, two further UMC 0.13 implementations of a DCO consisting of 64 AND–OR elements were analysed by post-layout gate-level simulations. In the first variant, no additional constraints have been defined and the standard cells were placed automatically. The placement of the second variant was performed by a TCL-script to ensure a regular placement of the AND–OR elements. For both placement methods, the routing was done with the autorouter of the Place&Route tool.

Fig. 19 shows the resulting layouts with AND–OR cells and Fig. 20 shows the simulated element delays for both variants (typical process, temperature and voltage). It can be seen that the automatic placement of the elements results in irregular physical arrangement and routing, thus, causing large delay variations between several consecutive DCO elements. By using the script-based placement, the standard deviation of the delay times has been reduced from 11.9 ps in the unconstrained layout to 5.6 ps without increasing the implementation effort.

4.6. Comparison with recent designs

Further measurement data are summarized in Table 1. As can be seen, most parameters are comparable or superior to recent examples. In addition, the described architecture is fully synthesizable. For example, re-synthesizing the 0.35 μm architecture in 0.13 μm and adjusting the multiplication factor for the new application took three man-days. The residual jitter is still high, but entirely sufficient for the target application.

5. Conclusion

We present an ADPLL design optimized for portable data logging and processing systems. The design achieves a fast multiplication factor adjustment to enable dynamic low power

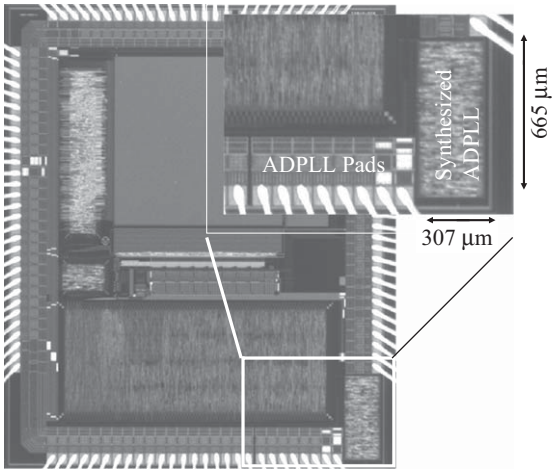

Fig. 21. Chip microphotograph of the 0.35 μm PLL (lower right corner) realized as part of a preprocessing pixel sensor SoC (backdrop).

Table 1
Performance comparison: described PLLs and recent literature.

Parameter	Proposed ADPLL		[1]	[4]	[14]
Process	0.35 μm CMOS	0.13 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.35 μm CMOS
Area	0.204 mm^2	0.027 mm^2	0.019 mm^2	0.16 mm^2	1.7 mm^2
Approach	Cell-based synthesizable	Cell-based synthesizable	Cell-based, mixed analog/digital DCO	Cell-based, mixed analog/digital DCO	Analog
Power dissipation	41 mW at 274 MHz	7.4 mW at 500 MHz	100 mW at 500 MHz	15 mW at 378 MHz	115 mW
Max. lock time	<8 cycles	<8 cycles	<272 cycles	<75 cycles	–
Output range	22.1–274 MHz	84–800 MHz	140–1030 MHz	2.4–378 MHz	80 MHz
Supply voltage	3.3 V	1.5 V	3.3 V	1.8 V	3.3 V
Peak–peak jitter	1000 ps	870 ps	143 ps	208 ps at 134.7 MHz	72.7 ps
Mult. factor	1-65536	1-255	–	4-13888	8

modes, wide range of multiplication factors to compensate for off-the-shelf reference clocks, and low power consumption. Long-term clock precision with respect to reference signal is assured, and the design is based entirely on digital standard cells for easy portability across different CMOS technologies. A chip micro-photograph of the 0.35 μm PLL on an SoC IC is shown in Fig. 21.

In [15], a method for fast PLL lock acquisition is presented which achieves lock times comparable with our successive approximation. However, the design in [15] relies on analog models of the DCO chain, which have to be coded into the frequency regulation algorithm, obstructing portability of this design across changing technologies. In contrast, the successive approximation used herein is in keeping with a technology-independent design, since it relies on ordinary clock cycle counter functionality to achieve its frequency lock.

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