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Exploiting Memristive $BiFeO_3$ Bilayer Structures for Compact Sequential Logics

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Resistive switching devices are considered as one of the most promising candidates for the next generation memories and nonvolatile logic applications. In this paper, $BiFeO_3$:Ti/$BiFeO_3$ (BFTO/BFO) bilayer structures with optimized BFTO/BFO thickness ratio which show symmetric, bipolar, and nonvolatile resistive switching with good retention and endurance performance, are presented. The resistive switching mechanism is understood by a model of flexible top and bottom Schottky-like barrier heights in the BFTO/BFO bilayer structures. The resistive switching at both positive and negative bias make it possible to use both polarities of reading bias to simultaneously program and store all 16 Boolean logic functions into a single cell of a BFTO/BFO bilayer structure in three logic cycles.

1. Introduction

Nonvolatile reconfigurable logic will allow researchers to develop compact, low-power devices and systems approaching brain-like intelligence.[1–5] The new hardware for basic logic computing should be integratable into silicon technology, and possess well defined state variables in large scale applications and low power consumption. It is well known that resistive switching devices can be integrated into large arrays for use as nonvolatile memory, analog or digital logics, sensors, and other applications that use resistance instead of voltage or charge as the physical state variable.[6,7]

Memristors are two-terminal passive devices which have been predicted theoretically as the fourth basic circuit element by L. O. Chua in 1971.[8] It was only in 2008 that the researchers from Hewlett-Packard Laboratories[9,10] revealed the missing link between resistive switching and memristors. In addition to being used in the next generation nonvolatile memories, the memristor is also a promising candidate to extend Moore's law beyond physical limits and implement beyond von-Neumann computing because only one memristor is needed to compute and store basic logic functions simultaneously in comparison to conventional CMOS (complementary metal-oxide-semiconductor) logic circuits that generally need much more components to realize the basic logic functions[3,7] and physically separate processing and memory operations.[11] There have been many reports on the realization of Boolean logic functions with bipolar resistive switches (BRS) and with complementary resistive switches (CRS).[12–21] However, so far not all 16 Boolean logic functions could be realized with a single BRS or CRS. In 2009, J. J. Yang et al.[4] proposed a family of memristively switched reconfigurable devices which exhibit transitions between pairs of four current-transport end-states, namely shunted rectifier, forward rectifier, reverse rectifier and head-to-head rectifier, by strictly controlling the initial distribution of oxygen vacancies in the TiO_2 layer, and predicted that these unique devices may allow new nanoelectronic architectures in the fields of memory, logic,

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and synaptic computing. However, the reproducibility of the experimental current-voltage data is poor (Figure 3 in another work),[4] and the related devices were found to switch ON and OFF at low voltage bias with longer time constants[10] which may cause the resistive switching degradation by reading bias, so it is doubted whether the reported TiO_2 devices are stable enough for the applications in universal memories or in non-volatile Boolean function computing devices which require high retention and endurance performance. Here, we propose to form a $BiFeO_3$:Ti/$BiFeO_3$ (BFTO/BFO) bilayer structure which shows typical nonvolatile bipolar resistive switching and new symmetric bipolar resistive switching by tuning the thickness of the BFTO layer without electroforming process. The using of both positive and negative reading bias in one resistive switching device is first reported, which makes it feasible to realize all 16 Boolean logic functions with a single symmetric bipolar resistive switching bilayer structure in three logic cycles. With a write-back step in the third logic cycle, the nonvolatile logic can be configured.

2. Results and Discussion

2.1. Fabrication and Electrical Characterization of BFTO/BFO Bilayer Structures

BFTO/BFO bilayer structures with different BFTO layer thicknesses have been fabricated on Pt/Sapphire substrates by pulsed laser deposition with sputtered circular Au contacts on top. The nominal thickness of BFO layer is 500 nm. The samples are labelled according to the nominal BFTO thickness of 50 nm, 100 nm, and 150 nm as sample-50, sample-100 and sample-150. The thickness and area of the Au top contacts are 30 nm and 0.045 mm^2, respectively. **Figure 1**a shows a typical cross-sectional bright-field TEM image of sample-100. There is no visible interface between BFTO and BFO at a distance of ca. 100 nm from the Pt bottom contact, which is likely due to the same lattice structure and similar lattice parameters for BFTO and BFO, and the potential diffusion of Ti which might occur to the surface of the BFTO layer in the negative temperature gradient during its preparation.[22] Applying energy-dispersive X-ray spectroscopy with a conventional Si(Li) detector in scanning TEM mode, Ti could be detected by area analysis neither above the Pt layer in the ≈100 nm thick BFTO region nor in the ≈600 nm thick BFTO/BFO range (not shown). This may be due to the low Ti content of nominal 1 at% in BFTO and to the substitutional incorporation of Ti into the BFTO lattice without Ti cluster formation.[23] There are some grain boundaries passing through the entire BFTO/BFO bilayer structure. These grain boundaries may trap oxygen vacancies and form conductive channels inside the BFTO/BFO film, which may provide a path for leakage current between BFTO and BFO layer.[10,24] Therefore, it is supposed that there is no electron barrier forming at the interface between BFTO and BFO. Figure 1b depicts a schematic sketch of the BFO/BFTO bilayer structures and the electric measurement configuration, which indicates that the electric measurements are carried out by a sourcemeter device and the bias voltage is applied between the

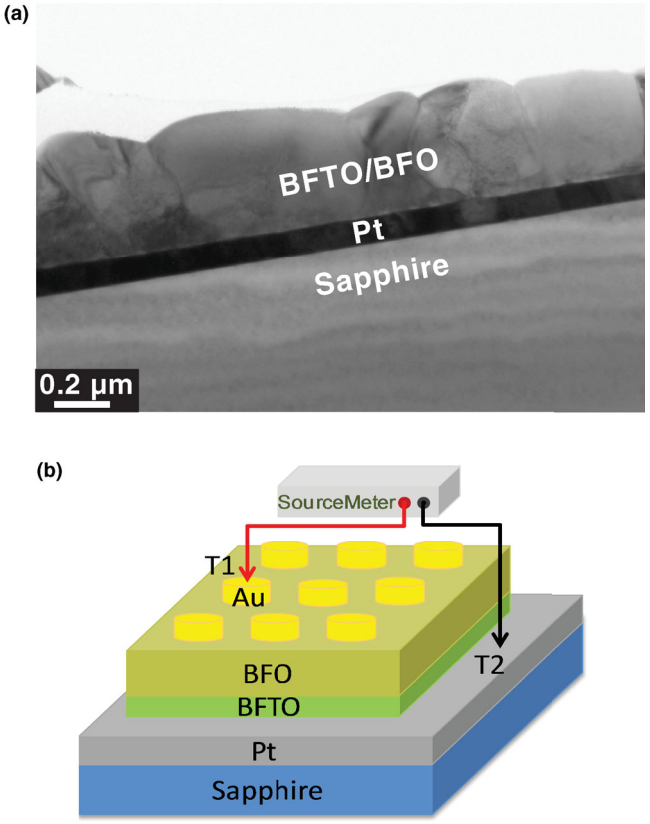

Figure 1. a) Cross-sectional bright-field TEM image of the as-prepared BFTO/BFO bilayer structure consisting of a nominal 100 nm thick BFTO layer on a 100 nm thick Pt layer on c-sapphire and a subsequently deposited BFO top layer with a nominal thickness of 500 nm. b) the schematic sketch of the BFTO/BFO bilayer structure and the electric measurement configuration.

Au top electrode (terminal T1) and the Pt bottom electrode (terminal T2). The Pt bottom electrode is grounded.

Figure 2a shows a sequence of ramping voltages, namely two positive triangular voltage sweeps followed by two negative triangular voltage sweeps. The voltage step is 0.4 V with the step time of 0.1 s. Figure 2b–d shows the current-voltage (*I*–*V*) curves of sample-50, sample-100, and sample-150, respectively. The numbers 1–16 label successive ramping voltages and the corresponding current branches in the *I*–*V* curves, and the arrows indicate the scanning direction of the applied ramping voltages. Sample-50 and sample-150 show typical bipolar resistive switching behavior without an electroforming step, in which the obvious hysteretic *I*–*V* behavior exists only for negative or positive ramping bias, respectively. However, in sample-100, the obvious hysteretic *I*–*V* behaviors exist in both negative and positive bias, which shows a symmetric bipolar resistive switching. After a positive writing bias the structure exhibits low resistive state in positive ramping bias (branch 2, 3, 4, 10, 11, and 12 in sample-100 and sample-150) and high resistance state only in the next negative ramping bias (branch 5 and 13 in sample-100 and sample-150), after a negative writing bias the structure shows low resistive state in negative ramping bias (branch 6, 7, 8, 14, 15, and 16 in sample-50 and sample-100)

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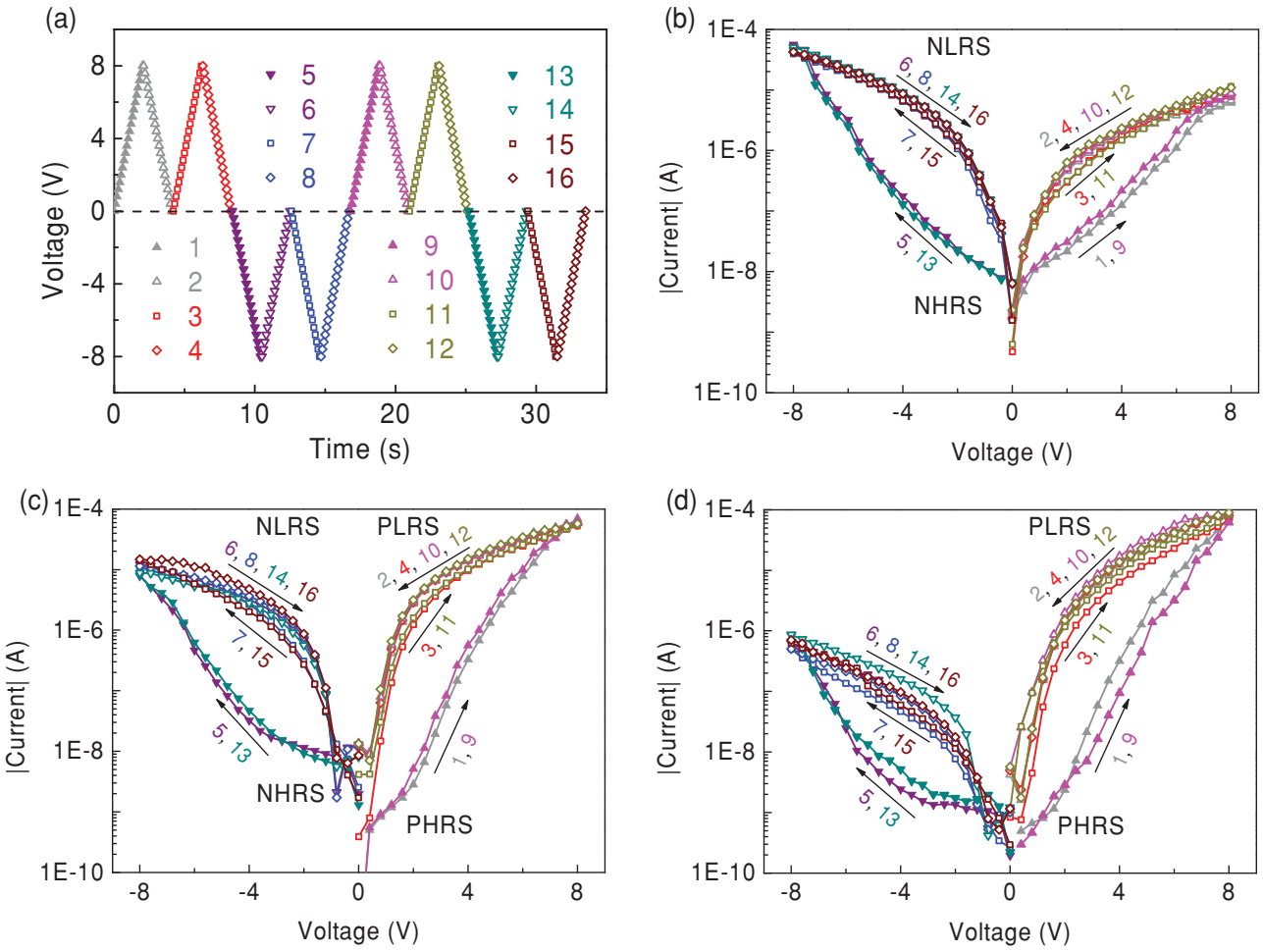

Figure 2. a) Sequence of ramping voltages. The numbers 1–16 label successive ramping voltages and the corresponding current branches on a logarithmic scale of b) sample-50, c) sample-100, and d) sample-150.

and high resistance state only in the next positive ramping bias (branch 1 and 9 in sample-50 and sample-100), which indicates the nonvolatility of the resistive switching. These *I*–*V* characteristics are quite stable as the *I*–*V* curves can be reproduced after 1 month (Supporting Information, Figure S1). The low resistance state and high resistance in positive ramping bias are abbreviated as PLRS and PHRS, respectively,[25] which are set and reset by positive writing bias and negative writing bias and read out by a positive reading bias. The low resistance state and high resistance in negative ramping bias are abbreviated as NLRS and NHRS, respectively,[25] which are set and reset by negative writing bias and positive writing bias and read out by a negative reading bias. The *I*–*V* curve of sample-100 suggests that both positive and negative reading bias can be used, and different resistance states can be obtained by different polarities of reading bias with the same writing bias.

2.2. Resistive Switching Mechanism in BFTO/BFO Bilayer Structures

In contrast to the abrupt current change with the formation and rupture of filaments,[26] here a rather gradually changing current is observed during resistive switching, which indicates the interface-mediated resistive switching in BFTO/BFO bilayer structures. The *I*–*V* characteristics with different Au contact area and the Au contact area dependent resistance value of different resistance states suggest that the resistive switching is induced by localized interface-mediated switching[26,27] (Supporting Information, Figure S2). In order to get further insight into the interface effect on the resistive switching, the *I*–*V* curves of sample-50, sample-100, and sample-150 in a small voltage range (from –2 V to +2 V) were measured in two different states, namely after applying a bias pulse of +8 V and after applying a bias pulse of –8 V for 0.1 s, which are shown in **Figure 3**a–c. The equivalent circuits corresponding to the bandstructure at different states are also presented in the right side of Figure 3 a–c. As shown in Figure 3a, the current of sample-50 is small in the both positive and negative voltage range after applying a positive bias pulse of +8 V, while a reverse rectification characteristic is observed after applying a bias pulse of –8 V. The equivalent circuit of sample-50 after applying a bias pulse of +8 V is a head-to-head rectifier which consists of two antiserially connected diodes (D_t and D_b) due to the Schottky-like contact (Φ_t and Φ_b) at both top (t) and bottom (b) interface and one resistor R_i denoting the bulk resistance of the BFTO/BFO

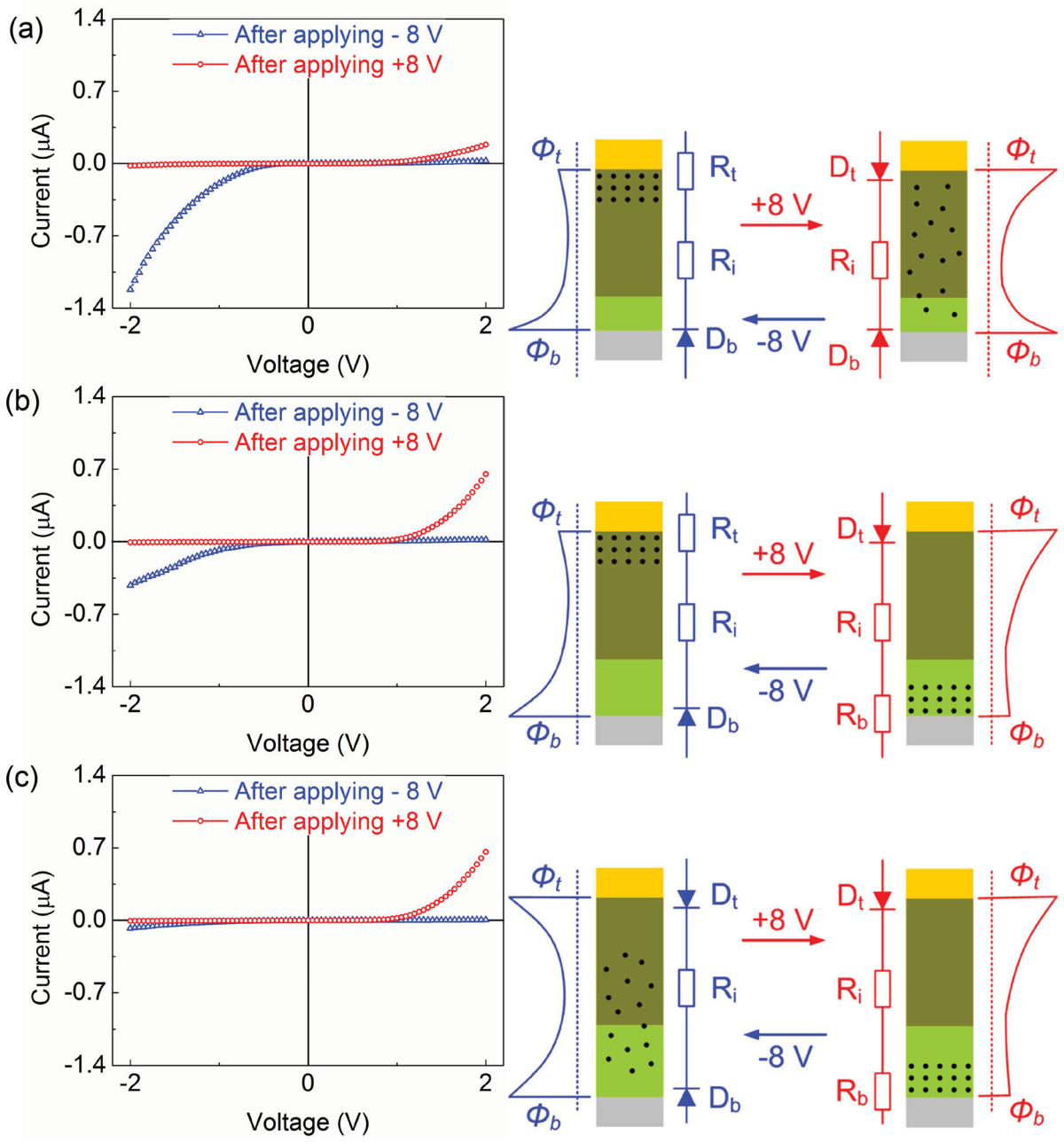

Figure 3. *I–V* curves from –2 V to +2 V of a) sample-50, b) sample-100, and c) sample-150 measured after applying a writing bias of +8 V and –8 V. The schematic band alignment between the top (t) electrode on BFO and the bottom (b) electrode on BFTO and the corresponding barrier heights (Φ_t and Φ_b), the distribution of the movable oxygen vacancies/ions (the black dots) and equivalent circuits are also indicated in the right side.

bilayer structure. The current is always blocked by one of the two Schottky-like interfaces regardless of the voltage polarity. After applying a pulse of –8 V, the Schottky-like barrier at the top interface decreases and the diode D_t turns into a resistor (R_t) whereas D_b remains a Schottky-like diode. The current is controlled by D_b and shows a reverse rectification characteristic. By applying a negative reading bias, D_b is forward biased and a large current flows (NLRS). A reverse phenomenon is observed in sample-150. The current is small at both positive and negative voltage range after applying a bias pulse of –8 V due to the head-to-head rectifier (D_t and D_b), and shows a forward rectification characteristic after applying a bias pulse of +8 V, which suggests that the Schottky-like barrier at bottom interface decreases and the Schottky-like diode at top interface (D_t) dominates the conductance. By applying a positive reading bias, D_t is forward and a large current flows (PLRS). While sample-100 demonstrates forward and reverse rectification characteristics after applying a bias pulse of +8 V and –8 V, respectively. This indicates the inversion between a reverse and a forward rectifier. After applying a pulse of +8 V, Schottky-like contact forms at top interface while Ohmic contact forms at bottom interface. The current is controlled by D_t. By applying a positive reading

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bias, D_t is forward biased and a large current flows (PLRS); by applying a negative reading bias, D_t is reversed and a small current flows (NHRS). After applying a pulse of –8 V, Ohmic contact forms at top interface while Schottky-like contact forms at bottom interface. The current is controlled by D_b, by applying a positive reading bias, D_b is reversed and a small current flows (PHRS); by applying a negative reading bias, D_b is forward biased and a large current flows (NLRS).

These results suggest that a flexible Schottky-like barrier forms at top interface and Schottky-like barrier forms at bottom interface in sample-50, Schottky-like barrier forms at top interface and flexible Schottky-like barrier forms at bottom interface in sample-150, while flexible Schottky-like barrier forms at both top and bottom interface in sample-100, and the flexible Schottky-like barrier plays an important role in the resistive switching of BFTO/BFO bilayer structures. The flexible Schottky-like barrier may come from the migration of charged oxygen vacancies/ions under the electric field of writing bias[4,10,28] and the redistribution of carriers with ferroelectric switching.[29,30] However, the BFTO/BFO bilayer structures do not show significant ferroelectric switching under the writing bias (Supporting Information, Figure S3), so the flexible Schottky-like barrier of BFTO/BFO bilayer structures is supposed to result from the migration of charged oxygen vacancies/ions. The devices were also found to switch faster with larger writing bias (for example, 10 µs at 20 V). This is consistent with the fact that the drift velocity of vacancies increases in a larger electric field,[31,32] which further confirms that the flexible Schottky-like barrier comes from the migration of charged oxygen vacancies/ions. The black dots in the right side of Figure 2 indicate the distribution of the movable oxygen vacancies/ions under the certain writing bias. The accumulation of charged oxygen vacancies/ions in the interface effectively reduces the corresponding Schottky-like barrier as BFO can be regarded as n-type semiconductor due to the naturally produced oxygen vacancies,[33,34] while the Schottky-like barrier is recovered when the charged oxygen vacancies/ions drift away from the interface. It is reported that BFO with a small concentration of Ti doping exhibits higher resistivity than pure BFO.[35,36] In sample-50, the BFO layer possesses larger resistance due to the thin BFTO layer, so that most of the applied voltage drops across the BFO layer. The active region[4] is the top BFO layer which possesses flexible Schottky-like barrier. With the increase of BFTO thickness, the BFTO layer becomes more resistive and most of the applied voltage drops across the BFTO layer which results in the active region forming only in BFTO layer in sample-150. In sample-100, the resistance of BFO and BFTO is comparable, and both BFO and BFTO layers are active regions, so the flexible Schottky-like barrier forms at both top and bottom interface.

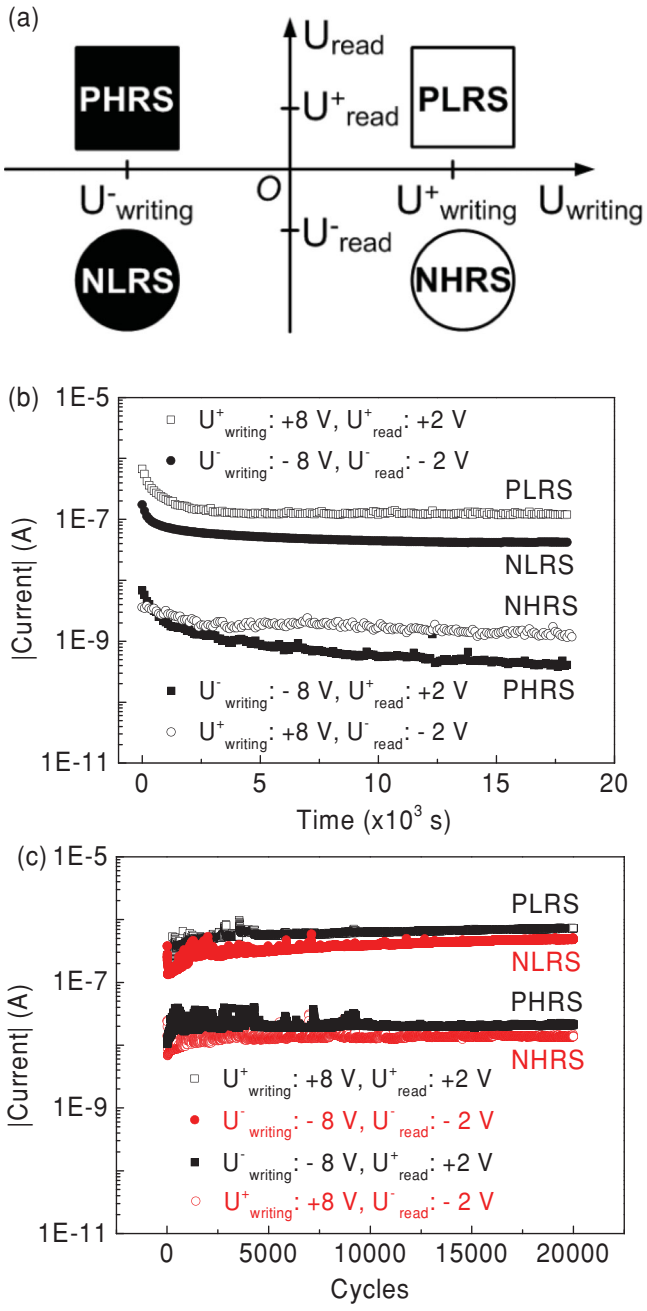

Figure 4. a) The relationship between the resistance states of sample-100 and the polarities of the applied writing bias $U_{writing}$ and the reading bias U_{read}. b) Retention tests of sample-100 with positive and negative reading bias. The writing and reading bias for the four independent measurements are indicated in the legend. c) Endurance tests of sample-100 with the reading bias of +2 V (black curve) and –2 V (red curve).

2.3. Nonvolatility of the Symmetric Bipolar Resistive Switching

In our previous work,[22,37–40] we have reported that a BFO single layer structures show typical bipolar resistive switching with excellent retention and endurance performance. In the following, we only present the nonvolatility of the symmetric bipolar resistive switching with sample-100.

Figure 4a reveals the relationship between the resistance state of sample-100 and the polarities of the applied writing and reading bias. If the writing and reading bias show the same polarity (both are positive or negative), the bilayer structure exhibits low resistance state (PLRS or NLRS), otherwise, the bilayer structure shows high resistance state (PHRS or NHRS). The resistance state of sample-100 is inverted by inverting

the polarity of the reading bias under the same writing bias. To check the nonvolatility of the states PLRS, PHRS, NLRS, and NHRS, retention tests were carried out by first applying a writing bias (+8 V or –8 V) and then repeating the reading bias (+2 V or –2 V) every 100 s. Generally, a current level detection is used as the resistance state detection for memristors and Figure 4b shows the current level detection results of PLRS, PHRS, NLRS, and NHRS. All PLRS, PHRS, NLRS, and NHRS show increasing resistance which may be caused by the redistribution of some charged oxygen vacancies/ions after the writing bias, however, PLRS and NLRS become stable after 5×10^3 s and 1×10^4 s, respectively. The low resistance state and high resistance state are still well defined after 1.8×10^4 s. The endurance properties with the positive and negative reading bias were also examined by repeating set/read/reset/read process for more than 2×10^4 cycles as shown in Figure 4c. The set/reset bias is +8 V or –8 V, and the reading bias is +2 V or –2 V. The PLRS, PHRS, NLRS, and NHRS in endurance tests show the same starting current values as for the retention tests and gradually increase until saturation due to Joule heating during the endurance tests. After 1×10^4 cycles, the read currents become stable, and the memory window is well kept after switching for 2×10^4 cycles. The low resistance state and high resistance state are distinguishable and it is expected that the stabilization and reliability of the resistance states can be further improved by Ar^+ irradiation.[38–40]

2.4. Realization of All 16 Boolean Logic Functions

In recent years, a concept of sequential logic[7,12,21] has been introduced to realize the logic functions in a sequential operation with a small set of resistive switching devices. E. Linn et al.[21] showed that a single BRS or CRS with write-back step can be used to realize 14 of 16 Boolean logic functions (except XOR and XNOR) in at most three sequential logic cycles. Sample-50 and sample-150 with typical bipolar resistive switching can be used to realize the 14 Boolean logic functions with negative and positive reading bias respectively. For the first time, we show that all 16 Boolean logic functions can be realized in three logic cycles with a single symmetric bipolar resistive switching BFTO/BFO bilayer structure cell in which the reading process can be used as an additional logic cycle. Furthermore, all 16 Boolean logic operations can be started with a same logic cycle, which is very favorable for practical applications. As an example, in the following we will explain how the Boolean logic function XOR can be programmed and stored into one BFTO/BFO bilayer structure cell.

Writing bias is determined by the potential of terminal 1 (*T1*) and terminal 2 (*T2*) which depend on the logic variables *p* and *q* (1 for high potential and 0 for low potential). Note that when *T1* and *T2* are at the same potential (*T1* = 0 and *T2* = 0 OR *T1* = 1 and *T2* = 1), no potential difference exists across the device, the state of the device is unchanged. As mentioned above, with the same writing bias the output is different by using different reading bias. Therefore, the output is defined by T1, T2, initial state of the device (*S'*) and reading bias (*r*) which are deemed to be the input variables. For the output, we assign the low resistance states PLRS and NLRS as logic "1" and the high resistance states PHRS and NHRS as logic "0". Because the state of the device is either state {PLRS, NHRS} or state {PHRS, NLRS}, state {PLRS, NHRS} can be assigned to 1 and state {PHRS, NLRS} can be assigned to 0. Similarly, positive reading bias is assigned to 1 and negative reading bias is assigned to 0. In **Table 1**, 16 possible combinations for these four input variables (*T1*, *T2*, *S'*, and *r*) and the corresponding output (Out) are listed, the relationship between output and input variables can be summarized by this equation:

Table 1. 16 possible combinations for the four input variables (*T1*, *T2*, *S'*, and *r*) and the corresponding output (Out). The equations indicate the relationships between output and the input variables.

T1	*T2*	*S'*	*r*	Out	Equation
0	0	1	1	"1"	$\mathrm{Out} = \left(T1 + \overline{T2}\right) \cdot S' \cdot \overline{r}$
1	0	1	1	"1"	
0	1	1	1	"0"	
1	1	1	1	"1"	
0	0	1	0	"0"	
1	0	1	0	"0"	
0	1	1	0	"1"	$\mathrm{Out} = \left(\overline{T1} \cdot T2\right) \cdot S' \cdot \overline{r}$
1	1	1	0	"0"	
0	0	0	1	"0"	
1	0	0	1	"1"	
0	1	0	1	"0"	$\mathrm{Out} = \left(T1 \cdot \overline{T2}\right) \cdot \overline{S'} \cdot r$
1	1	0	1	"0"	
0	0	0	0	"1"	
1	0	0	0	"0"	
0	1	0	0	"1"	$\mathrm{Out} = \left(\overline{T1} + T2\right) \cdot \overline{S'} \cdot \overline{r}$
1	1	0	0	"1"	

$$\mathrm{Out} = \left(T1 + \overline{T2}\right) \cdot S' \cdot r + \left(\overline{T1} \cdot T2\right) \cdot S' \cdot \overline{r} + \left(T1 \cdot \overline{T2}\right) \cdot \overline{S'} \cdot r + \left(\overline{T1} + T2\right) \cdot \overline{S'} \cdot \overline{r} \quad (1)$$

In general, by initializing the initial state *S'* to 1 or 0 which can be easily realized by writing pulse (*T1* = 1, *T2* = 0) or (*T1* = 0, *T2* = 1), respectively, Equation 1 can be reduced to:

$$\mathrm{Out} = \left(T1 + \overline{T2}\right) \cdot r + \left(\overline{T1} \cdot T2\right) \cdot \overline{r} \quad (2)$$

or

$$\mathrm{Out} = \left(T1 \cdot \overline{T2}\right) \cdot r + \left(\overline{T1} + T2\right) \cdot \overline{r} \quad (3)$$

Based on Equation 2, the Boolean logic function XOR can be implemented by (*T1* = 0, *T2* = *q*) with *r* = *p* as shown in Equation 4.

Adv. Funct. Mater. **2014**,
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(a)

$p \oplus q$			C.HV1		C.HV2		C.LV
			T1	T2	T1	T2	R
p	q	s	1	0	0	q	p
0	0	0	{PLRS, NHRS}		{PLRS, NHRS}		NHRS='0'
1	0	1	{PLRS, NHRS}		{PLRS, NHRS}		PLRS='1'
0	1	1	{PLRS, NHRS}		{PHRS, NLRS}		NLRS='1'
1	1	0	{PLRS, NHRS}		{PHRS, NLRS}		PHRS='0'

C.HV1 C.HV2 C.LV

$p \oplus q$			C.HV1		C.HV2		C.LV
			T1	T2	T1	T2	r
p	q	s	0	1	1	q	p
0	0	0	{PHRS, NLRS}		{PLRS, NHRS}		NHRS='0'
1	0	1	{PHRS, NLRS}		{PLRS, NHRS}		PLRS='1'
0	1	1	{PHRS, NLRS}		{PHRS, NLRS}		NLRS='1'
1	1	0	{PHRS, NLRS}		{PHRS, NLRS}		PHRS='0'

C.HV1 C.HV2 C.LV

(b)

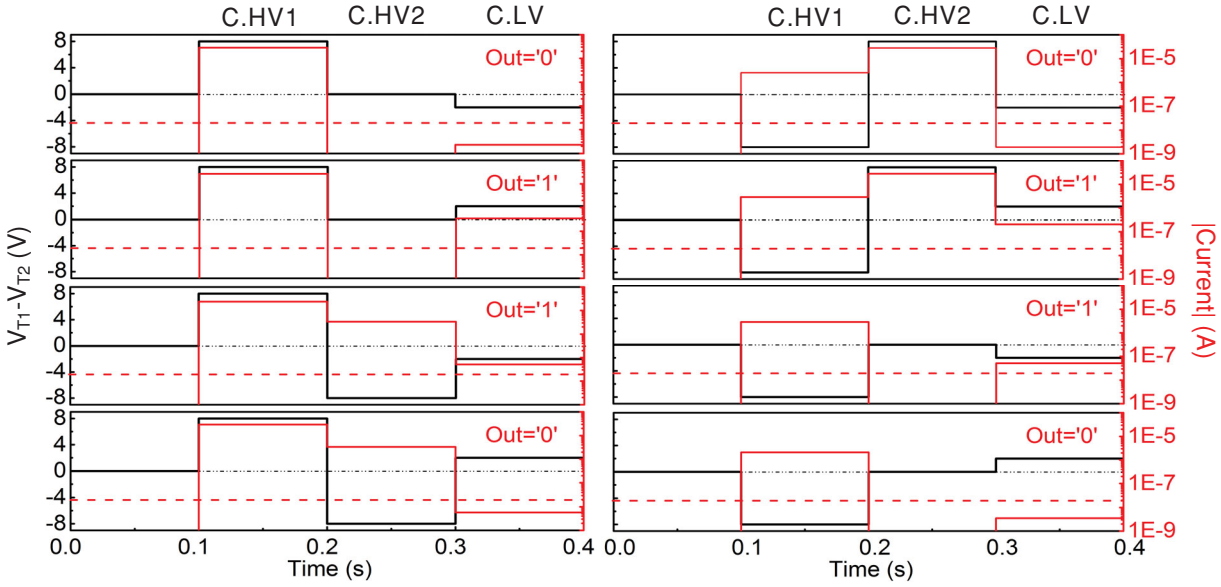

Figure 5. a) Logic operations for XOR with three logic cycles including two writing cycles C.HV1 and C.HV2 using ±8 V and one read cycle C.LV using ±2 V applied to the sample-100. b) The experimental demonstration of the sequential XOR for all four input states of p and q. The black and red curves display the applied potential between $T1$ and $T2$ (V_{T1}–V_{T2}) on a linear scale and the absolute value of the measured current on a logarithmic scale, respectively. The red dashed line is the current threshold level for Out = "0" and Out = "1", and the black dotted line is the zero-bias of V_{T1}–V_{T2}.

XOR is also possible by ($T1 = 1$, $T2 = q$) with $r = p$ based on Equation 3 as shown in Equation 5.

$$\text{Out} = p \text{ XOR } q = \overline{q} \cdot p + q \cdot \overline{p} = \left(0 + \overline{q}\right) \cdot p + \left(\overline{0} \cdot q\right) \cdot \overline{p} \quad (4)$$

$$\text{Out} = p \text{ XOR } q = \overline{q} \cdot p + q \cdot \overline{p} = \left(1 \cdot \overline{q}\right) \cdot p + \left(\overline{1} + q\right) \cdot \overline{p} \quad (5)$$

Figure 5a shows the realization of XOR with three logic cycles C.HV1, C.HV2, and C.LV (two writing cycles C.HV1 and C.HV2 and one reading cycle C.LV) and the corresponding experimental demonstrations with the prepared bilayer structure are shown in Figure 5b. Contrary to nonvolatile logics, the reading bias in the third logic cycle C.LV depends on the logic variable p (or q for the other Boolean logic functions). To accommodate nonvolatile logics, a write-back step in the third logic cycle C.LV can be used to store the output of the logic operations in the same device and make the reading bias independent of the input logic variables, which is not shown in Figure 5. For example, a positive and negative writing bias is applied in the write-back step to store the output 1 and 0 of the logic operations into the same device, respectively, and then both output 1 and 0 can be non-destructively read out by positive reading bias until next logic operation. Note that the write-back step is only performed in the third logic cycle C.LV for nonvolatile logics.

The other 15 Boolean logic functions can also be realized with three logic cycles (Supporting Information, Figure S4). The first logic cycle C.HV1 of all 16 Boolean logic operations can be a positive writing pulse and can be also a negative writing pulse. The nonvolatile logics can be realized by a write-back step in the third logic cycle C.LV. It is important to note that the high substrate temperature during thin film growth, the unstructured bottom electrode and the large thickness of BFTO/BFO bilayer structures do not necessarily compete the benefits of CMOS compatibility. We suggest to overcome these challenges by heating the sample surface during thin film growth using laser heating instead of using resistive heating, by structuring both the bottom and the top electrodes and by introducing well defined shunts into unstructured BFTO/BFO bilayer structures using Ar^+ ion irradiation.[40] There are other promising reports

on hybridizing CMOS with unstructured resistive switching TiO_2 layers.[3,41] Therefore, we consider unstructured BFTO/BFO bilayer structures with structured bottom and top electrodes as prospective building blocks for new micro/nano-electronic systems, for example, beyond von-Neumann computers.

3. Conclusions

In summary, BFTO/BFO bilayer structures have been fabricated. The bilayer structure with optimized BFTO/BFO thickness ratio shows nonvolatile bipolar resistive switching and symmetric bipolar resistive switching characteristics under both positive and negative bias. The high stability and reliability of LRS and HRS in symmetric bipolar resistive switching with positive and negative reading bias are examined by retention and endurance tests. By using the reading process as an additional logic cycle, the resistance state of symmetric bipolar resistive switching is inverted by inverting the polarity of the reading bias under the same writing bias, which makes it feasible to program all 16 Boolean logic functions into a single cell of a BFTO/BFO bilayer structure in three logic cycles. Nonvolatile logic is realized by a write-back step in the third logic cycle which stores the output of the logic operation until next writing cycle in the same cell of a BFTO/BFO bilayer structure. In the future, the BFTO/BFO bilayer structures can be integrated into crossbar circuits to achieve different arithmetic operations from single or cascaded cells (logic gates).

4. Experimental Section

Fabrication of BFTO/BFO Bilayer Thin Film Structures: To obtain a BFTO/BFO bilayer structure, a BFTO film with nominal 1 at% Ti was first deposited on Pt/Sapphire substrate, and then an undoped BFO film was deposited on the BFTO film without breaking vacuum and substrate heating by pulsed laser deposition (PLD). Approximately 5 min have been used to rotate the BFO target to the sputter position and to stabilize the system. The laser energy, laser repetition rate, oxygen ambient pressure, and growth temperature are 2 J cm^{-2}, 10 Hz, 13 mTorr, and 650 °C, respectively. The nominal thicknesses of BFTO layer are 50 nm, 100 nm, and 150 nm for sample-50, sample-100, and sample-150, respectively; and the thickness of BFO layer was kept at 500 nm. Following BFTO/BFO deposition, circular Au top contacts with an area of 0.045 mm^2 and a thickness of 30 nm were fabricated by DC magnetron sputtering at room temperature using metal shadow mask.

Characterization: Bright-field transmission electron microscopy (TEM) imaging as well as energy-dispersive X-ray spectroscopy (EDXS) in the scanning TEM mode was performed in cross-sectional geometry of sample-100 by means of an image-corrected FEI Titan 80–300 microscope. The current–voltage (*I*–*V*), the retention and endurance characteristic curves were measured by the two-probe method with a Keithley 2400 sourcemeter at room temperature under the dark condition.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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