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# A Model Based Comparison of BiFeO3 Device Applicability in Neuromorphic Hardware

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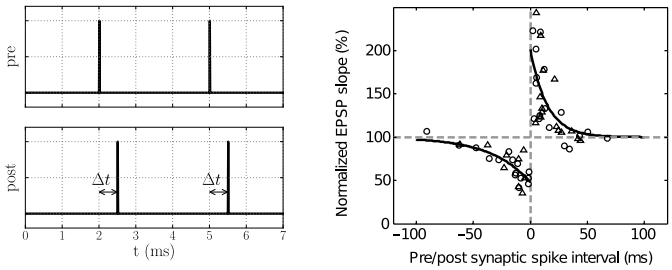
***Abstract*—Two terminal devices with switchable resistance have been of interest to electrical engineers for a long time, but only in the last few years these have attracted widespread attention. Recently a $BiFeO_3$ (BFO) capacitor-like metal-insulator-metal (MIM) structure was proposed as a synthetic synapse in neuromorphic systems, implementing voltage waveform driven spike timing dependent plasticity (STDP). Using a new device model that faithfully reproduces measurements of BFO-MIM structures we analyze how the switching characteristic affect the STDP learning window. Our simulations indicate that the gradual increase in the resistance change of BFO MIM structures result in a robust STDP with a biologically realistic learning window, whereas a distinct threshold followed by a steep hysteresis curve produce a narrow learning window and inflict strict operating conditions. Therefore we conclude that the steepness of the current voltage hysteresis curve is a fundamental characteristic to consider when designing synthetic synapses for neuromorphic hardware.**

***Index Terms*—neuromorphic systems, STDP, device model, memristive device, memristor**

## I. Introduction

The synapse is widely thought to be one key structural component of the brain, it acts as the connection point for neurons as they communicate through action potentials. The weight of the synapse regulates how well one neuron (presynaptic) transmits to another neuron (postsynaptic). It has been shown that if the postsynaptic neuron fires an action potential after the presynaptic neuron the weight is increased and vice versa. This dynamic is called spike timing dependent plasticity (STDP) and is considered as one of the underlying mechanisms for information processing and memory storage in biological neural networks [1]. Illustrated in Fig. 1 is how presynaptic spikes and excitatory postsynaptic potentials (EPSP) interact to form a learning window where the weight is changed.

In neuromorphic engineering one goal is to mimic the distributed computation of neural networks, with the underlying idea to access the evidently powerful computational paradigms of the brain. Another area where neuromorphic hardware may prove advantageous is as interface for live tissue, in these applications the critical aspect is not speed; but high levels




(a) (b)

Fig. 1. (a) Illustration of the spike timing concept: $\Delta t := t_{pre} - t_{post}$ ($= 0.5$ ms). (b) Measurements by Froemke and Dan [2] for the timing interval where the EPSP changes, thus displaying the learning window for the synaptic weight.

of integration, low power consumption and real-time behavior [3]. Since a single neuron on average can have $10^3$ to $10^4$ synaptic connections one of the major area consumers on a neuromorphic chip are the synapses, therefore it is important to implement the synapses in an area efficient way.

The last years have seen an increase of interest in two-terminal resistive switching devices (by some called memristors) from the neuromorphic engineering community [4]. As the synapse has a weight with continuous range a two-terminal non-volatile multilevel storage element would be an important part in neuromorphic hardware [5]. These devices can be realized in a crossbar fashion processed on top of standard semiconductor technology, achieving a high degree of integration [6]. Recently we demonstrated that $BiFeO_3$ (BFO) devices have the ability to faithfully reproduce the STDP phenomena [7]. Though many other devices have been proposed to form synaptic arrays, some may not be preferable in biologically feasible schemes for analog processing [6], [8]. In fact, our thesis is that devices aimed at digital storage are inherently ill suited in some situations, and we will discuss one fundamental property of synthetic synapses that affects voltage waveform driven STDP in neuromorphic hardware. The paper is organized as follows: section II contains an overview of physical

devices with focus on a BFO device, section III addresses the modeling of said device, in section IV practical model implementations for electrical simulations are compared and lastly conclusions are presented in section V.

## II. BFO Device Properties

For our research we use BFO thin films on a $Si/SiO_2/Pt$ substrate with a large-scale Pt bottom electrode and circular Au-top electrodes [9]. This capacitor-like BFO structure exhibits an IV hysteresis with inner state and threshold behavior. This means that in a small voltage range from about $-1.5\,\mathrm{V}$ to $2\,\mathrm{V}$, depending on the specific structure, an applied bias induces a state dependent current but does not significantly change the actual state. The BFO provides what we call a smooth switching over a wide voltage range with rectifying behavior and nearly linear correlation when in saturation (Fig. 2a). The device state can be programmed nearly arbitrarily and the process is reversible. The temporal behavior restricts the usage to real-time applications, because the time constants for saturation are $>1\,\mathrm{s}$ and a change in state requires programming periods of at least $1\,\mathrm{ms}$.

Fig. 2a shows a sample curve with the current for a given voltage $V_d$ over a $0.5\,\mathrm{mm}^2$ device. Also included for comparison are IV-curves of Ag/Si [5], $TiO_2$ [8] and Chalcogenide [10] capacitor like structures. From these reported measurements we can distinguish two fundamental types of characteristics; one where no significant resistance change is visible below a threshold voltage followed by a rapid switching to a low resistance state (Fig. 2c and 2d), and another where the smooth switching is evident (Fig. 2a and 2b). All these structure types has been associated with neuromorphic hardware and synapses [4], [5], [7], [8], [11], but as we shall see in the following sections the abrupt switching restrain the possibilities of a realistic STDP.

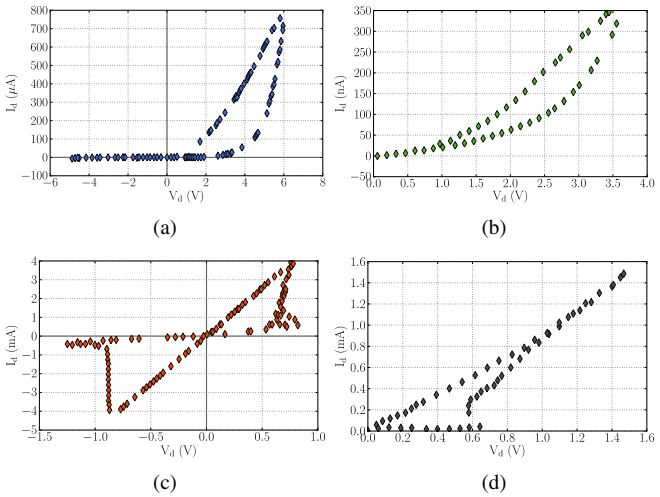



Fig. 2. IV characteristics of reported measurements from different capacitor-like structures that have been proposed for use in neuromorphic hardware: (a) $BiFeO_3$[7], (b) Ag/Si [5], (c) $TiO_2$ [8], (d) Chalcogenide (PCM) [10]

## III. Modeling

In order to develop a model for BFO, we used a voltage-saturation experiment. In this experiment the device was first reset and then programmed to high resistance state by applying successive $1\,\mathrm{V}$ steps, each held for $10\,\mathrm{s}$. An exponential saturation of the measured time-dependent current can be observed after every $1\,\mathrm{V}$ step and the level of this saturation increases exponentially with each step (Fig. 3). That is, we have two exponential dependencies, one is the state development over time (saturation) and the other is at which level the conductance will be limited for a given voltage.

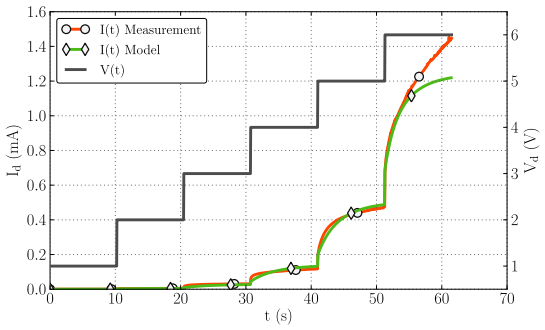



Fig. 3. Measured and modeled time-dependent current for 1 V voltage steps, each held for 10 s.

The IV characteristics are modeled as a system of equations with a non-linear ordinary differential equation of first order for the state variable $G$ and a distinction of cases for positive and negative voltages. The conductance of the current-voltage relationship can be interpreted as having three parts; the state dependent variable with two parasitic resistors expressed through $r_s$ and $g_p$. The voltage dependent limit of the state variable $G_{\mathrm{Lim}}$ is a simple exponential function and the saturation follows the basic principle $\dot{G} = a \cdot (G_{\mathrm{Lim}} - G)$. For a positive bias the logarithm function restricts the derivative to non-negative values, as where for negative voltages the exponential acts as threshold. The complete system of equations can be described with the formulas given in Eq. 1.

$$
\begin{aligned}
G_{\mathrm{Lim}}(V) &= g_{\mathrm{min}} + a_g \cdot e^{b_g V} \\
\frac{\mathrm{d}G(V,\ t)}{\mathrm{d}t} &= \begin{cases} \frac{a_p}{b_p} \cdot \ln\left(1 + e^{b_p (G_{\mathrm{Lim}}(V) - G)}\right), & V > 0 \\ a_n \left(e^{-b_n V} - 1\right) \left(G_{\mathrm{Lim}}(V) - G\right), & \text{else} \end{cases} \\
I(V,\ t) &= \begin{cases} k_p V^{e_p} \left(\frac{1}{G(t)^{-1} + r_{\mathrm{sp}}} + g_{\mathrm{pp}}\right), & V > 0 \\ k_n V^{e_n} \left(\frac{1}{G(t)^{-1} + r_{\mathrm{sn}}} + g_{\mathrm{pn}}\right), & \text{else} \end{cases}
\end{aligned}
$$

Eq. 1. System of equations of our device model with state variable $G$, voltage dependent limit $G_{\mathrm{Lim}}$ and current $I$.

Many models are mainly time controlled using a windowing function to limit a state variable between fixed values [12], [13] with partly very abrupt behavior which suits some types of devices. The voltage dependent limit in our model do however provide the ability to set a wide range of analog values and allows for robust simulations where small changes in either time or voltage levels only have little influence. Not

TABLE I
FITTED MODEL PARAMETERS

| | | | | | |
|---|---|---|---|---|---|
| $g_{\min}$ | $5 \times 10^{-3}$ | $a_p$ | $250 \times 10^{-3}$ | $e_n$ | 3 |
| $a_g$ | $30 \times 10^{-3}$ | $b_p$ | 15 | $g_{\text{pp}}$ | $1 \times 10^{-3}$ |
| $b_g$ | 1.2 | $a_n$ | $15 \times 10^{-6}$ | $g_{\text{pn}}$ | $500 \times 10^{-6}$ |
| $k_p$ | $3.7 \times 10^{-6}$ | $b_n$ | 3.1 | $r_{\text{sp}}$ | $50 \times 10^{-3}$ |
| $k_n$ | $20 \times 10^{-6}$ | $e_p$ | 1.8 | $r_{\text{sn}}$ | 200 |

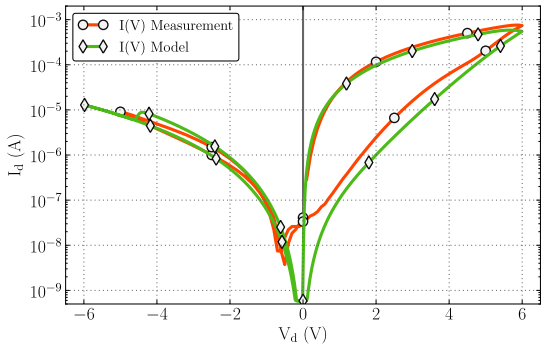



Fig. 4. Comparison of measured and modeled IV characteristics.

included in the model are effects of higher order, in particular the behavior in absence of any external bias and parasitic effects like capacitance or the influence of aging.

Even though the device model is fairly simple, it matches several IV characteristics, with time scales ranging from a few milliseconds to several seconds. Fig. 3 and 4 show the result with manually fitted parameters for a specific capacitor-like BFO structure. The same parameters were also used for following simulations and are listed in TABLE I.

## IV. SPICE IMPLEMENTATIONS

One way of operating a synthetic synapse is by the concept of waveforms that depending on timing will give rise to higher or lower voltages over a device [14]. Our implementation of this is depicted in Fig. 5 where pre- and postsynaptic spikes are represented by a negative voltage pulse ($V_{\text{pos|neg,min}}$) with a positive swing ($V_{\text{pos|neg,max}}$) followed by an exponential decay towards zero [7]. Due to the exponential decay the bias superposition of $V_{\text{pos}}$ and $V_{\text{neg}}$ will result in a larger positive or negative voltage proportional to the timing of the pulses. This can of course be generalized to a 'low' and a 'high' voltage that is centered around a common mode voltage other than zero.

For plausible electrical simulation we have implemented the before mentioned BFO device model in a SPICE (Simulator Program with Integrated Circuit Emphasis) dialect called Spectre®. As customary, our SPICE implementations make use of a behavioral current source which integrates the state variable as a voltage upon a virtual capacitor [12]. To investigate our thesis that the steepness of the switching may affect the performance of gradual resistance change, we also implemented a general model proposed by Yakopcic *et al.* [13]. The simulations for this device model were performed with the parameters given in Fig. 5, [13, pp. 1438], which are fitted to measurements performed on a $TiO_2$-device by Yang *et al.* [11], while our model was fitted to measurements of a BFO-device. As can be seen in Fig. 6 the resulting output exhibit the distinctive characteristic of a sharp and fast switching (Fig. 6a) compared to a smoother hysteresis curve of the BFO-device model (Fig. 6b).

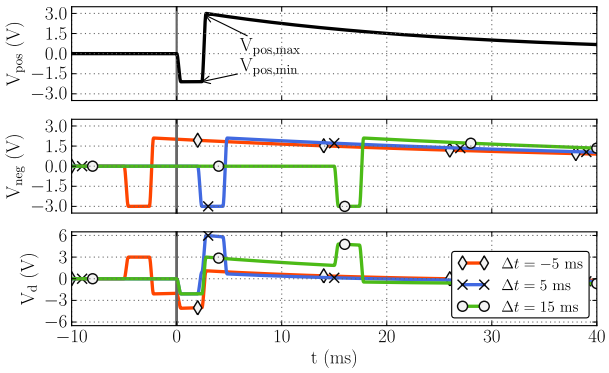



Fig. 5. Simulation of voltage waveforms using SPICE. If the $V_{\text{neg}}$ pulse occurs before or after the $V_{\text{pos}}$ pulse, $V_{\text{d}}$ would become largely negative or positive, respectively.

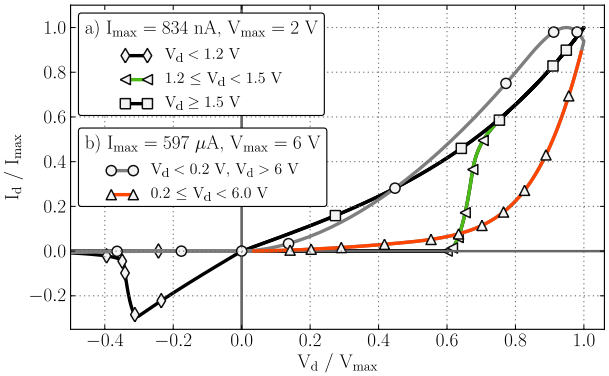
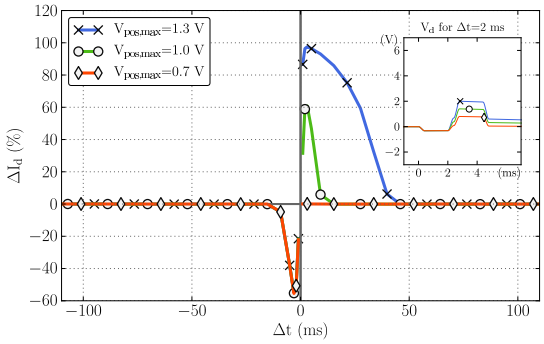


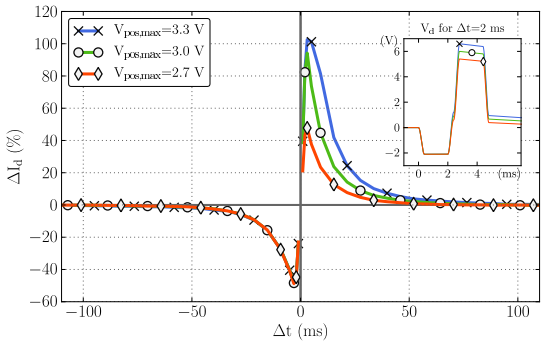

Fig. 6. Normalized SPICE simulations for an implementation of the the device model proposed by Yakopcic *et al.* 2011 [13] (a) and of our device model (b).

To simulate the Yakopcic model for STDP we adapted the voltage ranges to fit within the switching region of the $TiO_2$ device ($1.2 < V_{\text{d}} < 1.5$, Fig. 6). The impact of the different hysteresis characteristics is significant, as seen in Fig. 7a the sharp switching behavior gives rise to a narrow operating region where STDP is possible. As soon as the voltage over a device drops below the switching threshold, STDP would no longer be possible since the conductance cannot change. If we instead consider the upper bound of the switching region; pulses here will very rapidly change the resistance, leading to a condition where the learning window bulges and the risk is that the device reaches its maximum conductance prohibitively quick (even for a large $\Delta t$). In contrast we can observe that the smooth switching of the BFO produces a STDP that is robust to voltage variations (Fig. 7b). From this comparison we can surmise that a sharp switching device results in a

region of a few hundred millivolts where STDP is possible and small fluctuations could render the device nonfunctional as a synthetic synapse.




(a)




(b)

Fig. 7. STDP simulations of the implemented SPICE models, for each $\Delta t$ a sequence of 60 pulses has been used to change the conductance. The waveforms used were adapted for the voltage range of the respective model, in (a) for the $TiO_2$ device model and in (b) for our BFO device model.

## V. Conclusions

We have proposed a device model that is developed on a concept that differs from the frequently used window functions seen in literature [4]. Instead of limiting the state (effectively the conductance) between fixed values [12], our device model lets the upper limit vary depending on the applied voltage, which is required to capture the fact that BFO has a wide switching region. Simulations show that this model can give a good match to measurements; and as we have recently demonstrated this BFO-device can reproduce biologically realistic STDP [7].

Using the developed model we have shown that the device hysteresis characteristic plays a crucial part with regards to implementing synthetic synapses operated by the STDP paradigm using voltage waveforms. More specifically, a very steep switching characteristic leads to a narrow operating region useful for STDP, such a device would impose stricter restrictions on the creation of the used waveforms compared to a device with a smooth hysteresis. Because precise voltages require complex circuitry to deal with mismatch and process variations, this leads in the end to fewer neurons per chip. In a digital encoded memory it is advantageous to have a very steep switching characteristic since one strive to have well defined ones and zeros; ending up somewhere in between when performing a write is erroneous. In a neuromorphic memory on the other hand (i.e. the synaptic array), it is not only desired to have intermediate states, it is necessary; and a wide region of operation where these intermediate states can be written is the foundation for a robust reproduction of learning rules like STDP. Even though we have shown that BFO is highly interesting as a synthetic synapse the ultimate proof of BFO applicability in neuromorphic hardware would be to demonstrate this type of capcitor-like structure in a crossbar array on top of standard semiconductor technology. This will be the focus of future work.

## Acknowledgment

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## References

[1] W. Gerstner and W. Kistler, *Spiking Neuron Models: Single Neurons, Populations, Plasticity*. Cambridge University Press, 2002.

[2] R. Froemke and Y. Dan, "Spike-timing-dependent synaptic modification induced by natural spike trains," *Nature*, vol. 416, pp. 433–438, 2002.

[3] Giacomo Indiveri, *et al.*, "Neuromorphic silicon neuron circuits," *Frontiers in Neuroscience*, vol. 5, no. 00073, 2011.

[4] Robert Kozma, Robinson E. Pino, and Giovanni E. Pazienza, *Advances in Neuromorphic Memristor Science and Applications*. Springer, 2012.

[5] Sung Hyun Jo, Ting Chang, Idongesit Ebong, Bhavitavya B. Bhadviya, Pinaki Mazumder, and Wei Lu, "Nanoscale Memristor Device as Synapse in Neuromorphic Systems," *Nano Letters*, vol. 453, no. 10, pp. 1297–1301, April 2010.

[6] Kuk-Hwan Kim, Siddharth Gaba, Dana Wheeler, Jose M. Cruz Albrecht, Tahir Hussain, Narayan Srinivasa, and Wei Lu, "A Functional Hybrid Memristor Crossbar-Array/CMOS System for Data Storage and Neuromorphic Applications," *Nano Lett. 2012*, pp. 389–395, December 2011.

[7] C. Mayr, P. Stärke, J. Partzsch, L. Cederström, R. Schüffny, Y. Shuai, N. Du, and H. Schmidt, "Waveform Driven Plasticity in BiFeO3 Memristive Devices: Model and Implementation," in *Neural Information Processing Systems*, December 2012.

[8] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," *Nature*, vol. 453, no. 7191, pp. 80–83, May 2008.

[9] Y. Shuai, S. Zhou, D. Burger, M. Helm, and H. Schmidt, "Nonvolatile bipolar resistive switching in Au/$BiFeO_3$/Pt," *J. Appl. Phys.*, vol. 109, no. 12, p. 124117, 2011.

[10] Agostino Pirovano, Andrea L. Lacaita, Fabio Pellizzer, Sergey A. Kostylev, Augusto Benvenuti, and Robert Bez, "Low-Field Amorphous State Resistance and Threshold Voltage Drift in Chalcogenide Materials," *IEEE Transactions on Electron Devices*, vol. 51, May 2004.

[11] J. J. AU Yang, M. D. Pickett, X. Li, OhlbergDouglas A. A., D. R. Stewart, and R. S. Williams, "Memristive switching mechanism for metal//oxide//metal nanodevices," *Nature Nanotechnology*, pp. 429–433, July 2008.

[12] Z. Biolek, D. Biolek, and V. Biolková, "SPICE model of memristor with nonlinear dopant drift," *Radioengineering*, vol. 18, no. 2, pp. 210–214, 2009.

[13] C. Yakopcic, T. Taha, G. Subramanyam, R. Pino, and S. Rogers, "A Memristor Device Model," *Electron Device Letters, IEEE*, vol. 32, no. 10, pp. 1436 –1438, oct. 2011.

[14] B. Linares Barranco and T. Serrano Gotarredona, "Exploiting memristance in adaptive asynchronous spiking neuromorphic nanotechnology systems," in *Nanotechnology, 2009. IEEE-NANO 2009. 9th IEEE Conference on*, july 2009, pp. 601 –604.