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Novel implementation of memristive systems for data encryption and obfuscation

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With the rise of big data handling, new solutions are required to drive cryptographic algorithms for maintaining data security. Here, we exploit the nonvolatile, nonlinear resistance change in $BiFeO_3$ memristors [Shuai *et al.*, J. Appl. Phys. **109**, 124117 (2011)] by applying a voltage for the generation of second and higher harmonics and develop a new memristor-based encoding system from it to encrypt and obfuscate data. It is found that a $BiFeO_3$ memristor in high and low resistance state can be used to generate two clearly distinguishable sets of second and higher harmonics as recently predicted theoretically [Cohen *et al.*, Appl. Phys. Lett. **100**, 133109 (2012)]. The computed autocorrelation of encrypted data using higher harmonics generated by a $BiFeO_3$ memristor shows that the encoded data distribute randomly. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4869262]

I. INTRODUCTION

Big data handling has already begun to realize a number of benefits from cloud storage over traditional storage methods.[1–6] For example, cloud storage does not require installation, maintenance, or capital spending and it offers economies of scale that reduce overall storage costs. However, cloud storage users still encounter several challenges when performing large data transfers, including long transfer times, security exposure, and difficulties synchronizing data. Big data handling is turning to "on-the-wire" encryption as a first line of defense. This includes technologies like Secure File Transfer Protocol (SFTP) and File Transfer Protocol Secure (FTPS).[7] The big data handling has been inspired by a biological brain's approach to make sense of visual information and it has been suggested that new memristor-based cognitive systems can be used for big data handling.[8,9] With the reproducible fabrication of memristors, the exploitation of the new functionalities of memristive systems became possible. Namely, the functionalities of memristors are not confined to the emulation of the brain functions.[10] It has also been shown that the memristors can be used as nonvolatile resistive memories,[11–15] reconfigurable nonvolatile logic blocks,[16–18] artificial neural networks,[19–22] and as chaotic circuits.[22–24] This is just the beginning of exploiting the voltage-driven nonvolatile resistance changes of memristors. Thus, the memristor-based encryption would be a big advantage when working with memristive cognitive systems.

In memristor-based encryption, the authentication takes place with reference to the resistance state of the memristor and is part of the hardware. Hence, it is not susceptible to brute force attacks, malicious code, and hacking. Software-based encryption can cause bottlenecks that hinter a high security level. Furthermore, memristors can process data with much less power and with higher security level than today's software-based encryption systems. We are not aware of a work where memristor-based encryption and obfuscation have been investigated so far. After a short introduction, our work describes the experimental set-up and data analysis (Sec. II). The results of higher harmonics generation using memristors are discussed in Sec. III, and the higher harmonics generation of memristors being in high or low resistance state is analyzed in detail in Sec. IV. In Sec. V, we present a memristor-based implementation of a source encoding system for cryptographic applications and analyze the autocorrelation of input data and encrypted data. The paper is concluded in Sec. VI.

II. EXPERIMENTAL SETUP AND DATA ANALYSIS

Ferroelectric[25] and unipolar resistive switching[26,27] have been observed in polycrystalline $BiFeO_3$ (BFO) thin film. We have realized bipolar resistive switching BFO thin films on $Pt/Ti/SiO_2/Si$ substrates with large scale Pt/Ti bottom

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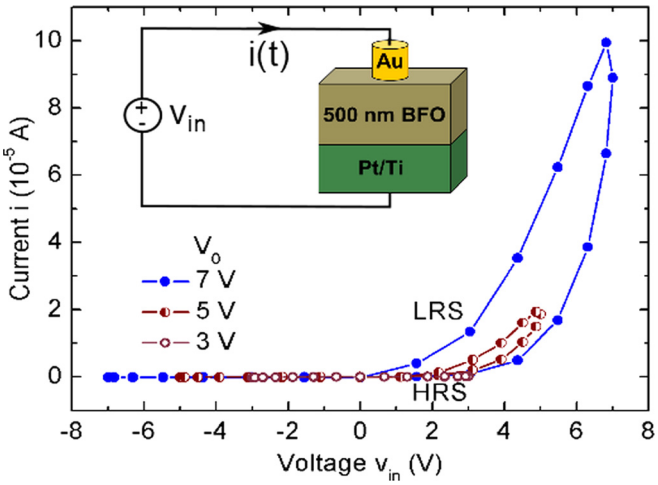

FIG. 1. Hysteretic current-voltage characteristics of a single layer Au/BFO/Pt memristor in LRS and HRS with a top electrode area of 0.217 mm^2 under sinusoidal source voltages $v_{in} = V_0 \sin(2\pi \cdot f1 \cdot t)$ with amplitudes $V_0 = 7$ V, 5 V, and 3 V. The inset shows the measurement circuit.

electrode and with circular magnetron sputtered Au top contacts.[1] The hysteretic current voltage (I–V) measurements have been carried out using a circuit, where the Au/BFO/Pt/Ti structure is connected directly with the source. The memristor is predefined in high resistance state (HRS) by using input pulse with amplitude −7 V before each measurement. As illustrated in Fig. 1, the I-V curve of a BFO memristor with a sinusoidal input voltage of $V_0 = 7$ V shows a repeatable hysteretic bipolar resistive switching. The BFO memristor is not completely switched into low resistance state (LRS) with the input voltage of amplitude 5 V. With input voltage of amplitude 3 V, the BFO memristor remains in high resistance state and works as a high resistive device with resistance in the gigaohm range. The high and low resistance state values of the BFO memristor are defined as the resistance values in the I-V curve at +2 V, when the BFO memristor is in HRS or LRS. For the BFO memristor with a 0.217 mm^2 top contact area, the resistance values in HRS and LRS amounts to 1188 MΩ and 13 MΩ ($R_{HRS}/R_{LRS} = 91.4$), respectively.

For the investigation of second and higher harmonics generation by using memristors,[28] we add a load resistor R_L into the circuit with a Keithley source meter (Fig. 2(a)) or a Lock-In Amplifier (Fig. 2(b)) as the input voltage source. The corresponding Keithley-setup (KL-setup) and Lock-In Amplifier-setup (LA-setup) are used to determine the power conversion efficiency (PCE). PCE is the ratio $P_{L,k}/P_S$

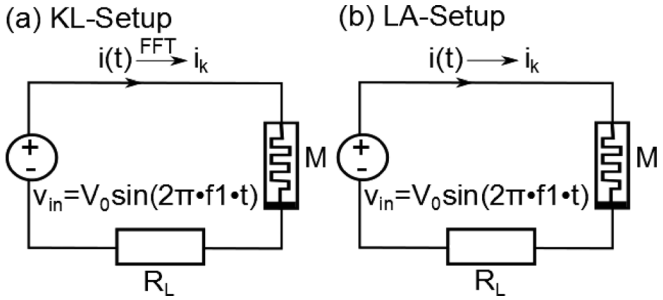

FIG. 2. Measurement circuit consisting of a memristor with memristance M, a load resistor R_L and (a) a 29 point sine wave as source and separately computed current i_k at different harmonics (KL-setup) or of (b) with a continuous sine wave as source and directly recorded current i_k (LA-setup).

between the power at kth harmonic $P_{L,k}$ and the average source power P_S. For the KL-setup (Fig. 2(a)), a Keithley 2400 is used to source a sinusoidal-like input voltage $v_{in}(t)$ over ten periods and to measure the current i(t). The Fourier transformation is then used to derive the current at different harmonics i_k (k = 1, 2, 3, 4).[29] For the LA-setup (Fig. 2(b)), a Lock-In Amplifier SR 830 is used to source a sinusoidal input voltage continuously and to measure the current i_k at different harmonics (k = 1, 2, 3, 4) directly.

Because of the pulse length restriction of the Keithley 2400 (pulse length of input voltage ≥0.1 s), the LA-setup is useful for analyzing the frequency dependence of the PCE for higher ground frequencies f1. The load resistor R_L works as a voltage divider and the PCEs are load resistor dependent.

III. RESULTS AND DISCUSSION

If we replace the memristor M in Fig. 2 by a linear resistor, it is predictable that the 50% of source power should be dissipated on the load resistor if the load resistor is equal to the constant resistor used. From the linear resistor measurement, we can see that 48.535% of the source power are dissipated on the load resistor and nearly no higher harmonics are generated. Furthermore, the maximum PCE at second harmonics amounts to only 0.015% and is negligible in comparison to the PCE $P_{L,k}/P_S$ (where k = 1, 2, 3, 4) obtained with a BFO memristor. In Fig. 3, the power ratios $P_{L,k}/P_S$ at different harmonics, which are obtained from BFO memristor, are represented as a function of load resistor R_L. In the lower load resistor range, the PCE curves of the load resistor under sinusoidal input voltage with frequency 0.357 Hz and

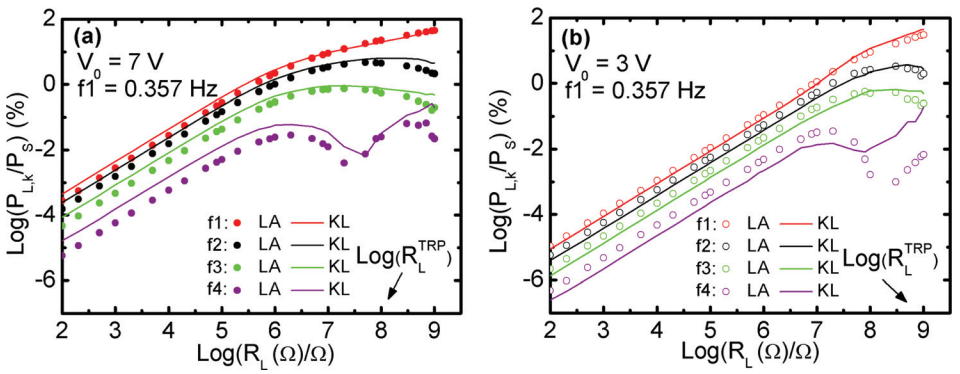

FIG. 3. PCEs at 1st–4th harmonics (red: f1, black: f2, green: f3, and violet: f4) for an input voltage $V_0 \sin(2\pi \cdot f1 \cdot t)$ with amplitudes (a) 7 V and (b) 3 V measured using the LA-setup (symbols) and KL-setup (lines) as a function of the load resistor R_L. The power ratios are recorded from BFO memristor ($R_{LRS} = 13$ MΩ, $R_{HRS} = 1188$ MΩ). The area of the top electrode is 0.217 mm^2. The transition point R_L^{TRP} is indicated by a small arrow.

TABLE I. PCEs at the transition point load resistor R_L^{TRP} under sinusoidal input voltage with amplitude 7 V, 5 V, and 3 V. The BFO memristor is preset in HRS before the PCE measurement. Note that for an input voltage of 3 V, the resistance state of the BFO memristor is not switched at all, i.e., the BFO memristor remains in HRS (Fig. 1).

V_0 (V)	$Log(R_L^{TRP})$ (1)	$P_{L,1}$ (%)	$P_{L,2}$ (%)	$P_{L,3}$ (%)	$P_{L,4}$ (%)	$\sum_{k=1}^{4} P_{L,k}$ (%)
7	8.100	17.990	6.330	0.725	0.001	25.046
5	8.360	20.130	4.320	0.470	0.002	24.922
3	8.699	21.110	2.810	0.330	0.002	24.252

amplitudes 7 V, 5 V (not shown), and 3 V depend linearly on the logarithm value of load resistor. In the higher load resistor range, the PCEs start to saturate. This is because that with larger load resistors R_L the input voltage mainly drops over the load resistor, and the BFO memristor is under voltage bias less than half of input source amplitude (around 3.5 V), and then the BFO memristor works as a gigaohm resistor as described in Fig. 1. Therefore, the generation of second and higher harmonics is depressed in the higher R_L range. Here, we define the transition point (TRP) of the PCE curves between the lower load resistor and higher load resistor range, and it is calculated as the average logarithmic value of the resistance R_{HRS} and R_{LRS}

$$Log_{10}(R_L) = \frac{(Log_{10}(R_{LRS}) + Log_{10}(R_{HRS}))}{2}. \quad (1)$$

The experimental maximum value of the PCE at 2nd harmonic amounts to 6.670% at a 300 MΩ load resistor (Fig. 3(a)). This value is smaller than the simulated maximum value of PCE at 2nd harmonic of a thin TiO_2 film which amounts to 16.9%.[2] However, both values are larger than the PCE at 2nd harmonic of a diode bridge frequency doubler, which amounts to 4.5%.[30] From Fig. 3, we can conclude that the results obtained with KL-setup and LA-setup agree with each other except for PCEs at 4th harmonic in the high load resistor range. This is due to the limited resolution of the LA-setup.

The PCE values of 1st, 2nd, 3rd, and 4th harmonics recorded under sinusoidal input voltage with amplitude 7 V, 5 V, and 3 V at corresponding TRPs are summarized in Table I.

The main part of the average power is dissipated across the load resistor only if the memristor is in LRS. If a BFO memristor with asymmetric I-V characteristics is used (Fig. 1), the sum of PCEs at TRP amounts to ca. 25%. It is also shown in Table I that the PCEs of second harmonic $P_{L,2}$ and third harmonic $P_{L,3}$ at TRPs increases and that the PCE $P_{L,1}$ decreases with increasing amplitude of input voltage, respectively. From that follows that under higher amplitudes less power is dissipated at ground frequency f1 across the load resistor as the generated harmonic power is higher.

The memristive device is fully switched with input voltage amplitude 7 V and can generate more harmonic power than the memristive device being only partially switched with 5 V and 3 V input voltage as shown for $P_{L,1}$ and $P_{L,2}$ in Fig. 4. From the differences in the power ratios being largest for an amplitude of 7 V, we conclude that the voltage-driven resistance state of the memristor strongly influences the power ratio of a given load resistor R_L. For cryptography and cryptanalysis, we suggest to use ca. 1–3 V large source amplitudes, which are comparable to the reading bias in BFO memristors[1] and will be sufficiently large to distinguish between the two sets of PCE of second and higher harmonics generated by the BFO memristor in HRS and LRS.

The hysteretic I-V characteristics of memristors can be asymmetric,[1] eight-like,[31] or peanut-like.[32,33] In the following, we analyze the PCEs of memristors with three different hysteretic I-V curves.

The I-V characteristics of the BFO memristor have been used to model memristive system with other I-V characteristics. Namely, the first period of the asymmetric I-V characteristics (Fig. 5(a)) has been used to model the first period of a symmetric I-V characteristics, i.e., eight-like hysteresis (Fig. 5(c)), and of a peanut-like hysteresis (Fig. 5(e)), by data mirroring and by data mirroring and rotation, respectively. The R_{HRS} and R_{LRS} for eight-like and peanut-like hysteresis are defined as resistance values at +2 V from the I-V curve, and the logarithm of both transition point load resistors R_L^{TRP} are 8.1 and are the same as the logarithm of the R_L^{TRP} of the asymmetric hysteresis (Fig. 5(a)). The PCE values at 2nd, 3rd, and 4th harmonics and ground frequency are listed in Table II. In the memristive system with symmetric I-V characteristics, the whole cycle power is dissipated on the load resistor and the sum of PCEs at the transition point load resistor amounts to 50%. As shown in Table II, it is clear that the PCEs at 2nd harmonic of eight-like and peanut-like hysteresis are around 1/18 (0.360/6.330) of the PCE at 2nd harmonic from an asymmetric memristive system. The PCEs at 3rd harmonic of a symmetric hysteresis

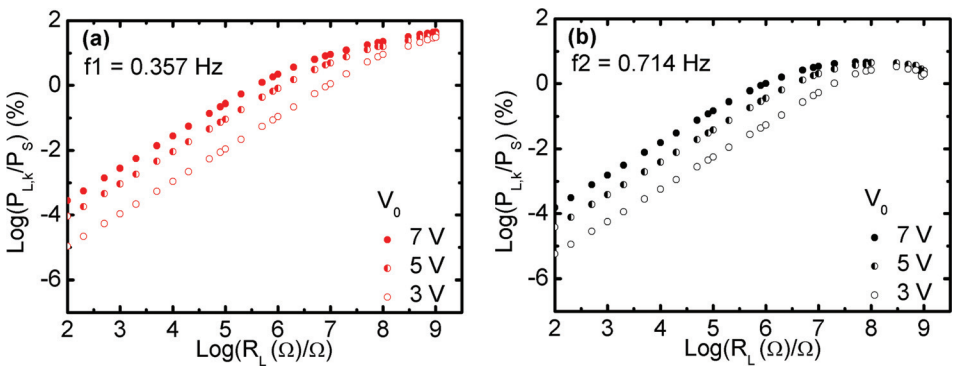

FIG. 4. PCEs of a BFO memristor on a logarithmic scale for input voltage with amplitudes 7 V, 5 V, and 3 V of the (a) ground frequency f1 (red) and (b) 2nd harmonic f2 (black) measured using the LA-setup as a function of the load resistor on a logarithmic scale.

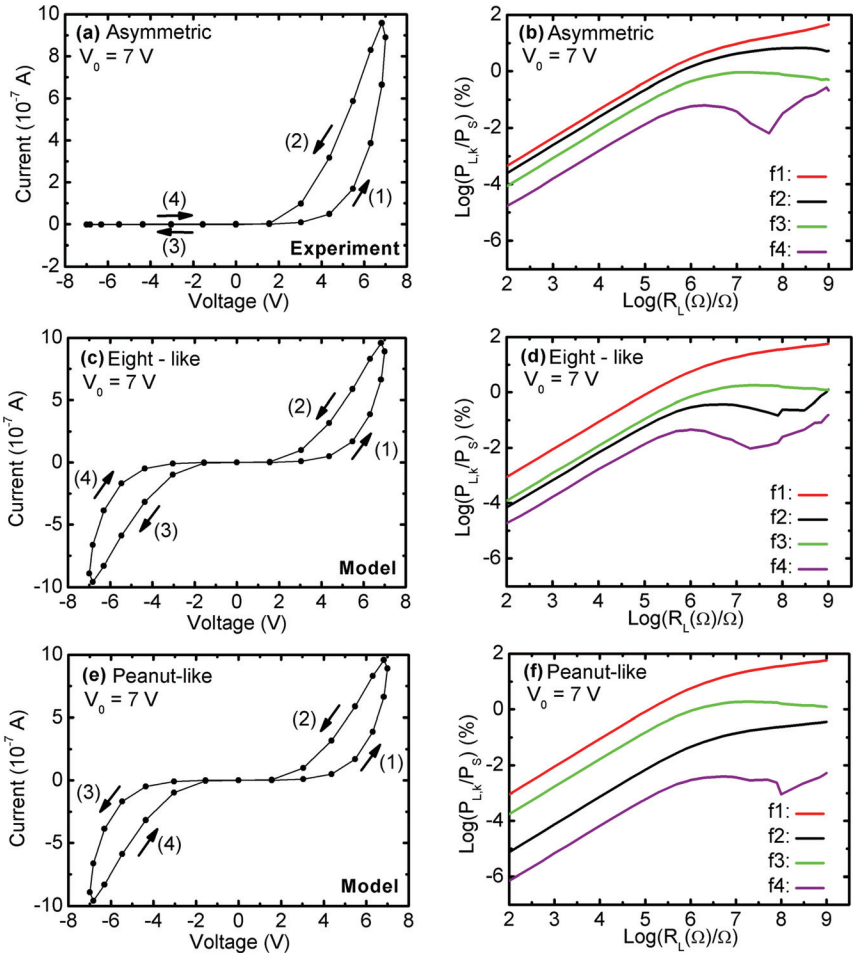

FIG. 5. PCEs (red: f1, black: f2, green: f3, and blue: f4) of a memristive device with (a) and (b) asymmetric, (c) and (d) eight-like, and (e) and (f) peanut-like hysteretic I-V characteristics. For this measurement, the KL-setup is used. The power ratios are measured as a function of the load resistor R_L with a sinusoidal input voltage at an amplitude of 7 V and a frequency of 0.357 Hz. The top contact area of the BFO memristor is 0.217 mm^2.

are more than three times larger than the PCEs at 3rd harmonic of the asymmetric hysteresis. From a mathematical point of view, it is because eight-like and peanut-like I-V characteristics suppress the even harmonics of the Fourier series, more power is distributed into odd harmonics, and memristors with symmetric I-V characteristics are useful for the generation of PCEs at 3rd harmonic.

IV. MULTIPLE HARMONIC GENERATION BY A BFO MEMRISTOR IN HIGH AND LOW RESISTANCE STATE

Before implementing BFO memristors in cryptography and cryptanalysis, one has to check whether a memristor in HRS and LRS generates different sets of higher harmonics. Single layer BFO memristors can be switched to LRS or HRS by applying a writing bias of +7 V or −7 V, respectively.[1] The power ratios are then measured under sinusoidal input voltage with amplitude 3 V with the sample remaining in LRS or HRS (Fig. 6).

If we have a closer look at the power ratio curves at 2nd harmonic in Fig. 7, for the same load resistor R_L, the PCE of the memristor in LRS is much higher than the PCE of a memristor in HRS. This is because the BFO memristor works as a diode in LRS, which is connected in series with a load resistor, and as a high-ohmic resistor in HRS (insets in Fig. 7). In our system, the maximum PCE value at 2nd harmonic in LRS is 4.072% at load resistor 800 kΩ and in HRS is 0.353% at load resistor 5 MΩ. Therefore, the two clearly distinguishable sets of power ratio curves at 2nd harmonic can be used for data encryption and obfuscation.

TABLE II. Calculated PCEs at the transition point load resistor R_L^{TRP} in series with a memristive device with asymmetric (experimental), eight-like (model), and peanut-like hysteretic (model) I-V characteristics at sinusoidal input voltage of 7 V.

I-V	$Log(R_L^{TRP})$ (1)	$P_{L,1}$ (%)	$P_{L,2}$ (%)	$P_{L,3}$ (%)	$P_{L,4}$ (%)	$\sum_{k=1}^{4} P_{L,k}$ (%)
Asymmetric	8.100	17.990	6.330	0.725	0.001	25.046
Eight-like	8.100	43.700	0.360	2.350	0.030	46.440
Peanut-like	8.100	43.700	0.360	2.470	0.003	46.533

V. DATA ENCRYPTION AND OBFUSCATION

The memristor-based encoding system is demonstrated in Fig. 8. We suggest to encode the input data in binary form (0, 1) by correspondingly switching the memristor (LRS and HRS). In our case, a writing voltage V_W of +/− 7 V is used to change the resistance state of the BFO memristors with respect to the input data, and a sinusoidal input voltage with amplitude 3 V is applied to the memristor in order to generate the higher harmonics from the corresponding memristance state. The multiplexer ensures that either the memristor state is written or a sinusoidal input voltage with writing bias V_W or the reading bias V_R is applied to the memristor (Fig. 8). As an example, here we use two sets of

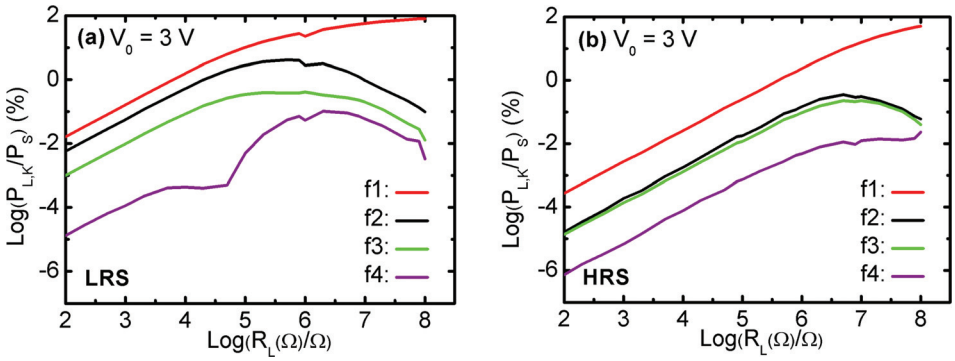

FIG. 6. PCEs of a BFO memristor in (a) LRS and (b) HRS under a sinusoidal input voltage with amplitude 3 V and ground frequency 0.357 Hz (f1 red: ground frequency, f2 black: 2nd harmonic, f3 green: 3rd harmonic, and f4 violet: 4th harmonic). The power ratios are measured in KL-setup in dependence on the load resistor. The sample is switched in LRS or HRS by applying a 0.1 s long writing pulse of +7 V or −7 V, respectively. The area of the top electrode is 0.089 mm^2.

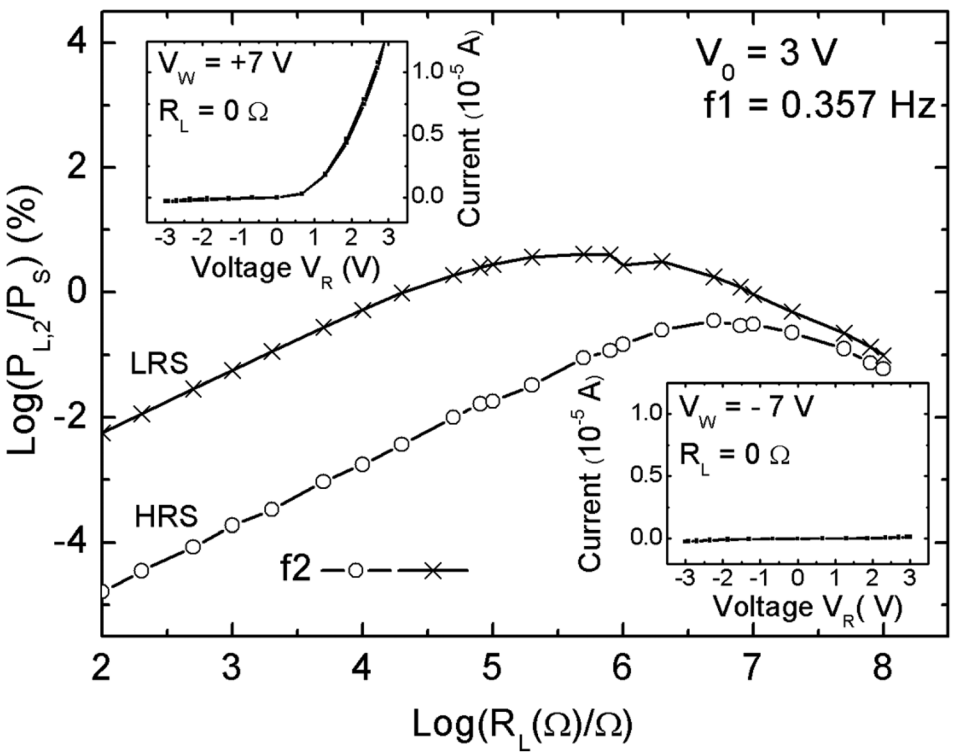

FIG. 7. PCEs at 2nd harmonic of a BFO memristor in LRS and HRS with sinusoidal input voltage with amplitude 3 V and ground frequency 0.357 Hz. The power ratios have been measured using KL-setup and are dependent on the load resistor. The sample is switched in LRS and HRS by applying a 0.1 s pulse of +7 V and −7 V, respectively. The top electrode area of the sample amounts to 0.089 mm^2. The insets show the I-V curves from the BFO memristor with a zero load resistor in the reading bias range where LRS and HRS remain unchanged.

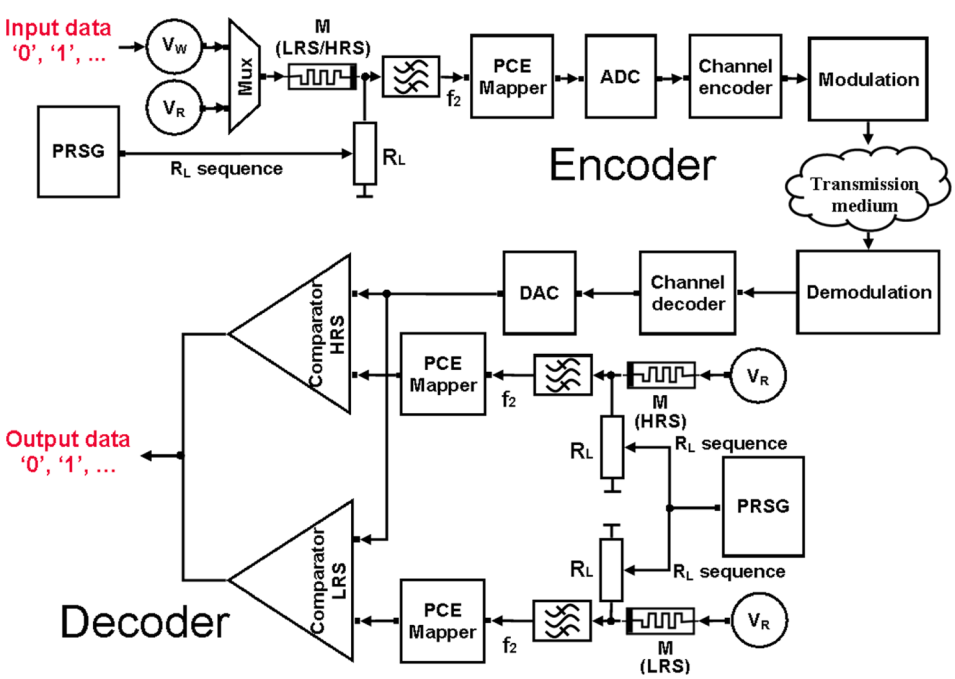

FIG. 8. Block diagram depicting a memristor-based source encoding system for data encryption and obfuscation.

2nd harmonics of a memristor in LRS and HRS to encrypt binary data "0" and "1," respectively. As shown before, the PCEs strongly depend on the resistance state of the memristor and on the load resistor in series with the memristor. In the demonstrated system, the load resistor values R_L are generated by a Pseudo Random Sequence Generator (PRSG)[34] for every input data bit because of its simple implementation and high speed performance. We suggest to subdivide the load resistor range into three parts. For PCE values at LRS ("0"), the load resistor values lie in the range from 0.100 kΩ to 4.570 kΩ (red arrow in Fig. 9), and for PCE values at HRS ("1") the load resistor values lie in the range from 0.030 MΩ to 1.995 MΩ (blue arrow in Fig. 9). The load resistor range between the load resistor range for LRS and HRS is labeled load resistor range for fixed points (FPs) (black arrow in Fig. 9).

When a data bit has to be transmitted on the encoder side (Fig. 8), the PRSG generates a value and a correspondingly selected load resistor value is obtained. If the bit to be transmitted is a "0" ("1"), the generated load resistor value lies in the LRS (HRS) load resistor range, and the corresponding PCE values of the load resistor will be transmitted, which can range between 1%–100%. Otherwise the input data is withheld and a zero value is transmitted. If the PRSG generates a load resistor value in the fixed point range, a zero value is transmitted. This ensures that there is no ambiguity to the receiver whether a data transmission was withheld or not. In total approximately 40% of the LRS and HRS load resistor values are used for encoding the LRS and HRS, respectively. In the encoding simulation, the load resistor R_L is represented by 9-bit binary data.

On the decoder side, the received data are first demodulated, decoded, and converted back to its analog form. The receiver also houses two BFO memristors (Fig. 8): one is always set to HRS and the other one to LRS. The PRSG at encoder and decoder are synchronized and have the same constraints. Therefore, the same random sequence of load resistors is generated at the encoder and decoder. The decoded data are fed to both comparators, if the output of the comparator with input from memristor in LRS is high, then data "0" is transmitted. If the output of the comparator with input from memristor in HRS is high, then data "1" is then transmitted. And if the output of both comparators is low, a fixed point was transmitted (Fig. 8). Different harmonics f_k and reading bias V_0 both at sender and receiver can be generated by additional PRSG for further upgrade of security level.

We put the total abstract text of this work into ASCII format and obtained a 6600 bit long sequence of data (0, 1). To test the randomness of the PCE values, we took the first 1217 input data (0, 1) out of the ASCII-encoded abstract text, set the memristor state (LRS, HRS), and generated the corresponding PCE values using the memristor in series with a randomly generated load resistor R_L. Finally, the PCE values have been transformed (1%–100%) by the PCE mapper (Figs. 9 and 10). In the following, the transformed PCEs are labeled "Mapped PCEs." In Fig. 10, (a) 1217 input data (0, 1) and correspondingly mapped PCEs (1%–100%) are shown versus the element number in R_L sequence. The R_L sequence has been generated using a PRSG. Because only load resistors in the LRS (HRS) range (Fig. 9) can be used to encode "0" ("1"), the element number in the R_L sequence which is needed for encoding the 1217 input data (0, 1) amounts to 3000.

The autocorrelation function a(j) of a data sequence z(m) at jth lag is defined as

$$a(j) = \frac{1}{N \cdot a(0)} \sum_{m=1}^{N-j} (z(m) - \bar{z})(z(m+j) - \bar{z}), \qquad (2)$$

where a(0) is the variance of the data sequence, $\bar{z}$ is the mean value of z(m), N is the computed data length, and j = 1, 2, 3,…, N − 1. Using Eq. (2), we calculated the autocorrelation

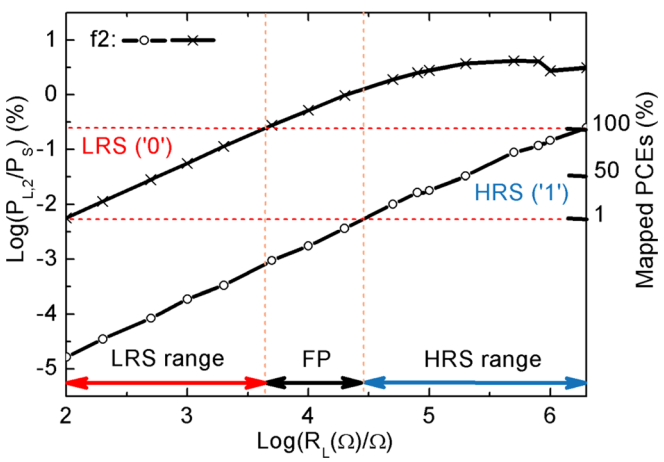

FIG. 9. Mapping of the PCEs at the 2nd harmonic versus load resistor R_L. Using a BFO memristor in LRS or in HRS in series with the load resistor R_L the PCE values have been generated. Note that we only use load resistors in the LRS (HRS) load resistor range to encode the input data "0" ("1""). For the BFO memristor, the LRS load resistor range (red arrow) and the HRS load resistor range (blue arrow) are separated by the FP load resistor range (black arrow).

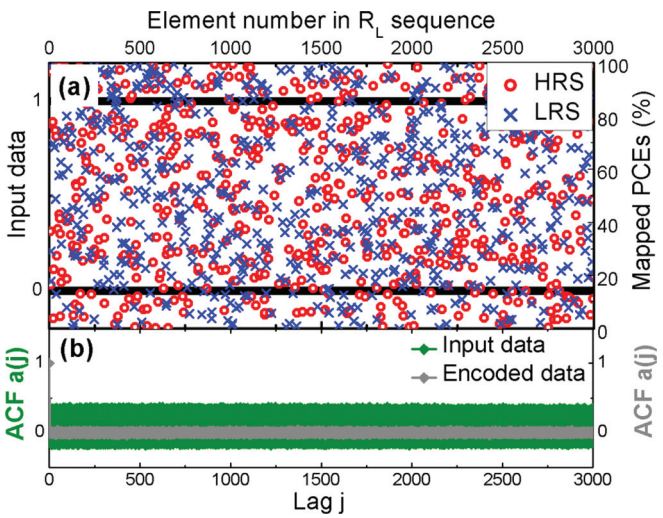

FIG. 10. (a) (left) 1217 input data (0, 1) versus randomly generated elements of load resistor R_L sequence of length 3000. The 1217 input data (0, 1) are taken out of the ASCII-encoded abstract text with a total sequence length of 6600. The mapped PCE values (1%–100%) are shown on the right axis. (b) Autocorrelation function a(j) of input data sequence (left axis) and of encoded data sequence (right axis). a(j) has been calculated using Eq. (2). Both data sequences (N = 12 170) have been repeated 10 times and are much longer than the maximum lag used (Lag < 3000).

function a(j) to test the randomness of data sequence. As shown in Fig. 10(b), the computed autocorrelation function (ACF) of the input data, which amounts to around 0.396, is much larger than the ACF of the encoded data, whose average value amounts to 0.018. The a(j) values suggest that the encoded data are randomly distributed.

VI. CONCLUSIONS

The efficient generation of second and higher harmonics has been demonstrated using a BFO memristor. It is concluded that the PCEs at 1st, 2nd, 3rd, and 4th harmonics not only depend on amplitude of the sinusoidal input voltage but also on the symmetry of the hysteretic current-voltage (I-V) characteristics of the memristor. For a given load resistor and sinusoidal input voltage, the power ratios of a memristor at 2nd harmonic with asymmetric hysteretic I-V curves are larger than the power ratios of a memristor with symmetric hysteretic I-V curves. We suggest to encode the input data in binary form (0, 1) by correspondingly switching the BFO memristor (LRS and HRS). Two distinguishable sets of harmonics are generated by a BFO memristor in LRS or HRS under sinusoidal input voltage with small reading amplitude. This can be used for a data transfer system with high data transfer security, reliability, and robustness. The security level of the system can be further increased by randomly choosing the input voltage V_R, the analyzed harmonics, the fixed point range of load resistors, and a memristor from an array of memristors. The temperature dependence of the encryption system is not considered in this work. Nevertheless, the power ratio values could be different if the encoder and decoder are working at different temperatures. Another issue is the low frequency of hardware-based encoding and decoding. If look-up tables are included, which alters the system into partially software-based encoding and decoding, the frequency of encoding and decoding can be significantly enhanced.

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