A current-mode conductance-based silicon neuron for Address-Event neuromorphic systems

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Abstract—Silicon neuron circuits emulate the electro-physiological behavior of real neurons. Many circuits can be integrated on a single Very Large Scale Integration (VLSI) device, and form large networks of spiking neurons. Connectivity among neurons can be achieved by using time multiplexing and fast asynchronous digital circuits. As the basic characteristics of the silicon neurons are determined at design time, and cannot be changed after the chip is fabricated, it is crucial to implement a circuit which represents an accurate model of real neurons, but at the same time is compact, low-power and compatible with asynchronous logic. Here we present a current-mode conductance-based neuron circuit, with spike-frequency adaptation, refractory period, and bio-physically realistic dynamics which is compact, low-power and compatible with fast asynchronous digital circuits.

I. INTRODUCTION

Many VLSI models of spiking neurons have been developed in the past [1]–[9], and many are still being actively investigated [10]–[13]. A common goal is to integrate large numbers of these circuits on single chips, or even full wafers, and create large networks of neurons, densely interconnected. In these systems, the strategy used to connect multiple neurons with each other is to use asynchronous digital circuits that map and route the spikes as they are generated to other neurons on different chips or other areas of the same chip/wafer [14], [15]. It is therefore crucial to develop compact low-power circuits, that implement faithful models of real neurons, but that can also produce extremely fast digital pulses required by the asynchronous circuits that manage the communication infrastructure.

A family of spiking neuron models that allows us to implement large, massively parallel networks of neurons is the Integrate-and-Fire (I&F) model. I&F neurons integrate pre-synaptic input currents and generate a voltage pulse analogous to an action potential when the integrated voltage reaches a spiking threshold. Networks of I&F neurons have been shown to exhibit a wide range of useful computational properties, including feature binding, segmentation, pattern recognition, onset detection, input prediction, *etc.*.

It has been recently argued however that simple I&F models do not produce a rich enough range of behaviors useful for investigating the computational properties of large neural networks, thus compromising the usefulness of ded-icated hardware implementations [13], [16], [17]. Wijekoon and Dudek recently proposed an alternative phenomenological VLSI model, loosely based on the Izhikevich model [16], which can produce a wide range of spiking patterns, using a very small number of transistors [13]. This circuit is also low power, but it operates in "scaled–time" (*i.e.* on microsecond scale, rather than millisecond scale). Therefore it cannot be used to implement artificial or hybrid systems that interact with the world in real–time. In addition both this phenomenological model, and the vast majority of I&F neuron circuits previously proposed do not exhibit conductance-based behavior, which is crucial for implementing bio-physically realistic models of neurons.

There is a class of VLSI conductance-based silicon neurons that has been proposed in the past [2], [6], [7]. These indeed implement faithful models of real neurons, but they use a considerable amount of silicon real-estate (*i.e.* many transistors and large capacitors). A new generation of bio-physically realistic circuits has been recently proposed [10], [11], which emulates the dynamics of neuronal proteic channels, repro-duces faithful action potential traces, and use a considerable lower number of transistors per neuron model. But these circuits do not produce fast digital pulses, and cannot be easily interfaced to asynchronous digital circuits.

We propose a phenomenological silicon neuron circuit, based on a variant of a low-power I&F model [18], which is conductance-based, compact, real–time (with bio-physically realistic temporal dynamics), and compatible with the asyn-chronous Address-Event Representation (AER) [19]. The cir-cuit uses a current-mode approach, similar to that proposed in [9], [12], but rather than using conventional log-domain filters [20], it uses the diff-pair integrator (DPI) [21] for im-plementing tunable dynamic conductances. The subthreshold log-domain circuits used in [9], [12] require p-FETs with isolated wells, while the DPI filters can be implemented using both n-type and p-type variants of the circuit, and can be designed with more compact layouts. An additional advantage of the DPI circuit over the standard current-mode log-domain circuit [20], is given by the possibility to control the circuit's gain with an additional independent bias voltage. A detailed analysis of both circuits and advantages of one over the other is presented in [22].
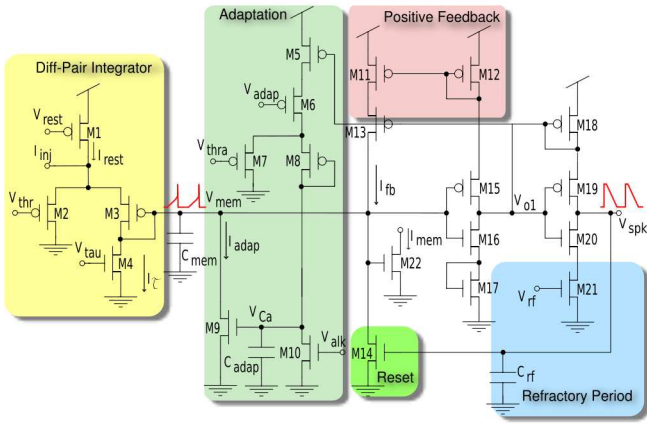
Fig. 1. Schematic diagram of the Differential-Pair Integrator (DPI) neuron circuit.

In addition to the conductance-based behavior, the circuit implements a series of functionalities which reproduce many important features observed in real neurons: a *positive-feedback* mechanism, which reproduces the effect of Sodium activation and inactivation channels in real neurons; a *refractory period* mechanism for limiting the maximum possible firing rate of the neuron; and a *spike-frequency adaptation* mechanism, which effectively introduces a second slow variable in the model, potentially allowing for subthreshold resonances and oscillatory behaviors [16].

The circuit's positive feedback mechanism drastically reduces the switching time of the neuron's MOSFETs, and makes the model extremely low-power. In the next Section we describe the circuit and explain its operational principles; in Section III we present experimental results; and in Section IV we draw the conclusions and describe future work on it.

II. THE SILICON NEURON CIRCUIT

The silicon neuron circuit schematic is shown in Fig. 1. The circuit comprises:

- An input DPI circuit [21] (M1-M4,M22), which models the neuron's leak conductance, and provides exponential subthreshold dynamics in response to constant input currents.
- An integrating capacitor C_{mem}, which represents the neuron's membrane capacitance.
- A second instance of a DPI (M5-M10), which models the neuron's Calcium conductance, and implements the spike frequency adaptation mechanism.
- An inverting amplifier (M15-M17) with positive feedback (M11-M13).
- A starved inverter with controllable slew rate (M18-M21), which can be used to set arbitrary refractory periods.
- The neuron's reset transistor (M14).

The read-out transistor M22 is used in simulations and for the analytical derivations, but was actually not included in the final layout of the circuit.

A. Circuit operation

The input current I_{inj} is summed to a constant background current (set by V_{rest}) which can be used to model spontaneous activity. Input currents are integrated by the DPI, increasing the membrane voltage V_{mem}. As V_{mem} approaches the switching voltage of the inverting amplifier, the feedback current I_{fb} starts to flow through M11-M13, increasing V_{mem} more sharply. This positive feedback has the effect of making the amplifier M15-M16 switch very rapidly, reducing dramatically its power dissipation. When V_{mem} increases enough to make the first inverter switch the voltage V_{O1} is brought to ground and V_{spk} is driven to V_{dd}. Then the membrane capacitor C_{mem} is discharged back to ground through the reset transistor M14, V_{O1} rises back sharply to V_{dd}, and the voltage V_{spk} is slowly reset to zero, at a rate controlled by the bias voltage V_{rf} and the size of C_{rf}. The neuron's refractory period lasts as long as V_{spk} is sufficiently high to keep the reset transistor on. During the spike emission period (while V_{O1} is low), a current with amplitude set by V_{adap} is sourced into the adaptation DPI, with a gain set by the gate bias voltage V_{thra}, and a time constant set by V_{alk}. The adaptation current I_{adap} increases with every spike, following the same first-order dynamics of I_{mem}. As a consequence, given the negative-feedback property of I_{adap}, the neuron's response to a step input current is characterized by an initial output firing rate proportional to the input current, which gradually decreases until an equilibrium is reached, thus reproducing the spike-frequency adaptation behavior observed in real neurons.

The subthreshold behavior of the neuron can be derived analytically, by assuming that the relevant transistors operate in the weak-inversion (or subthreshold) regime [23]. For this analysis we neglect the adaptation current I_{adap}, as this becomes non-negligible only after the first spike. In weak-inversion, the drain current of a saturated n-FET changes exponentially with its gate voltage [23]. In particular:

$$I_{mem} = I_0 e^{\frac{\kappa V_{mem}}{U_T}} \qquad (1)$$

where I_0 is the n-FET's leakage current, κ is the subthreshold slope factor and U_T is the thermal voltage [23]. The subthreshold branch current I_{M3} of the differential pair is given by:

$$I_{M3} = I_{in} \frac{e^{\frac{\kappa(V_{dd}-V_{mem})}{U_T}}}{e^{\frac{\kappa(V_{dd}-V_{mem})}{U_T}} + e^{\frac{\kappa(V_{dd}-V_{thr})}{U_T}}} \qquad (2)$$

where $I_{in} = I_{rest} + I_{inj}$. If we assume that the subthreshold slope coefficients κ of n and p-FETs are equal, we arbitrarily define $I_g \doteq I_0 e^{\frac{\kappa V_{thr}}{U_T}}$, and take into account eq. (1), we can rewrite I_{M3} as:

$$I_{M3} = I_{in} \frac{1}{1 + \frac{I_{mem}}{I_g}} \qquad (3)$$

Kirchhoff's current law on the V_{mem} node yields:

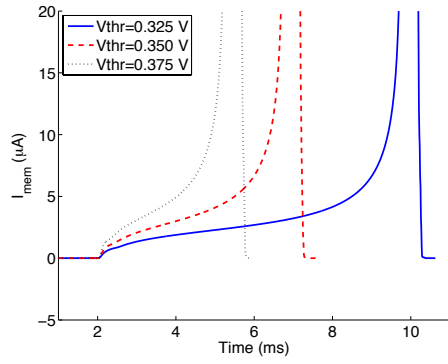$$C_{mem} \frac{d}{dt} V_{mem} = I_{M3} - I_\tau + I_{fb} \qquad (4)$$

Fig. 2. Silicon neuron membrane current I_{mem} in response to a constant step input current, for different values of the V_{thr} bias setting.

where $I_{fb} \approx I_{M16} = I_0 e^{\frac{\kappa^2}{\kappa+1}\frac{V_{mem}}{U_T}}$ and $I_\tau = I_0 e^{\frac{\kappa V_\tau}{U_T}}$.

If we differentiate eq. (1) with respect to V_{mem} and combine it with the eq. (4) we obtain:

$$\tau \frac{d}{dt} I_{mem} = -I_{mem} \left(1 - \frac{I_{M3}}{I_\tau} - \frac{I_{fb}}{I_\tau}\right) \qquad (5)$$

where $\tau \doteq \frac{U_T C_{mem}}{\kappa I_\tau}$. Replacing I_{M3} from eq. (3) into eq. (5) yields:

$$\tau \frac{d}{dt} I_{mem} + I_{mem}(1 - \frac{I_{fb}}{I_\tau}) = I_{in} \frac{\frac{I_{mem}}{I_{tau}}}{1 + \frac{I_{mem}}{I_g}} \qquad (6)$$

This is a first-order non-linear differential equation. However, for small values of V_{mem} (*e.g.* at the beginning of an action potential) the effect of the DPI dominates on the positive feedback, and we can neglect the current I_{fb}. Moreover, the right-hand term of eq. (6) can be reduced to $I_{in}\frac{I_g}{I_\tau}$, if $I_g \ll I_{mem}$. In these conditions eq. (6) simplifies to:

$$\tau \frac{d}{dt} I_{mem} + I_{mem} = I_{in} \frac{I_g}{I_\tau} \qquad (7)$$

Thus, for small values of V_{mem}, and sufficiently large values of I_{mem}, such that $I_{mem} \gg I_g$ the silicon neuron exhibits a classical RC-filter type behavior.

III. EXPERIMENTAL RESULTS

The results described here were obtained using SPICE simulations. However a small $4.45 \times 1.94 \text{mm}^2$ prototype chip, containing 32 of these neurons, has already been designed and fabricated using a 0.35μm AMS CMOS technology. The SPICE simulations were carried out using $0.35\mu m$ AMS process parameters and $3.3V$ power supply setting. In Fig. 2 we plot the transient simulations results, for a step input current and different settings of the V_{thr} bias parameter. There are two important aspects to note in this data. The first one is the RC profile of the membrane current I_{mem}, when the current is low; this effect is due to the charge phase of the DPI circuit and its response characteristic is clearly visible, until the effect of the positive feedback starts to dominate and
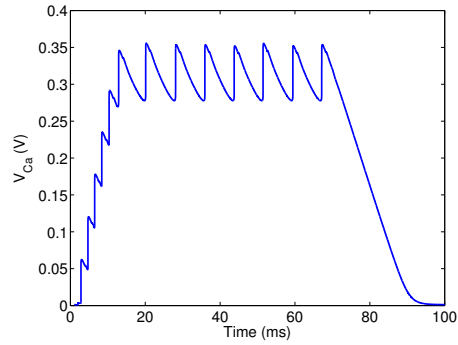
(a)
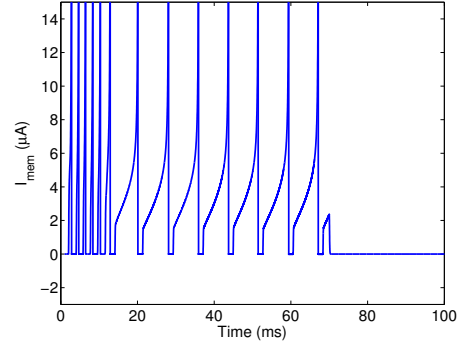
(b)

Fig. 3. Spike-frequency adaptation: (a) adaptation internal signal related to the Calcium concentration present in real neurons; (b) membrane "potential" signal traces in response to a step input current

finally generates a spike. The second aspect we would like to point out is the effect of the bias voltage V_{thr}: higher values of this bias increase the value of the DPI's steady state output, as predicted by eq. (7). The more this bias is increased, the more current is injected into the integrating capacitor C_{mem}, resulting in a sharper growing of the membrane current. A sharper increase of this current means that the V_{mem} voltage reaches the inverting amplifier's threshold voltage in a shorter time, resulting in an earlier spike generation. This can clearly be seen in Fig. 2, where the neuron membrane current I_{mem} is plotted for different values of the bias V_{thr}, in response to the same step input current.

As mentioned in Section I, an important feature of this circuit is the presence of a second, slower variable (*e.g.* V_{Ca}), which allows the circuit to implement a spike frequency adaptation mechanism. We activated the adaptation DPI (M5-M10) by decreasing the value of V_{adap} below V_{dd} and carried out transient simulations, observing the behavior of the neuron for multiple output spikes.

In Fig. 3(a) we show the V_{ca} voltage measured in these simulations: the voltage steadily increases with every spike, until it reaches an equilibrium, at which the neuron's output spike frequency is maximally reduced. In Fig. 3(b) we plot the membrane current I_{mem} as a function of time, measured in the same simulation run. As shown, the neuron's spike frequency

decreases as V_{Ca} increases, until the steady state is reached.

SPICE simulations were carried out also to evaluate the circuit's power dissipation characteristics. The digital spikes produced by the neuron (*e.g.* derived from the V_{O1} node) are extremely narrow, lasting about 300ns. The circuit's simulated average power consumption measured during this period is approximately 7pJ/spike. This measure is commonly used to describe circuit performance in the literature (*e.g.* Wijekoon and Dudek report 8.5pJ/spike [13]), and to our knowledge, this is the best figure ever reported. However, a more realistic measure is the *average* power dissipation measured during the whole current integration and action-potential generation phase. For example, given an average firing rate of 10Hz, the power dissipation should be measured over 100ms (*e.g.* from the end of one spike, to the end of the subsequent spike). In this case, the (simulated) average power consumption of our neuron circuit is approximately $267pJ$.

The power consumption specifications and other characteristics of the circuit, for the specific implementation made using a standard 4-metal, double-poly 0.35μm CMOS process, are summarize in Table I.

IV. CONCLUSIONS AND OUTLOOK

We designed and implemented a low-power current-mode conductance-based neuron circuit, with refractory period and spike frequency adaptation mechanisms. We described its properties by means of formal analysis and SPICE simulations. The results shown in each case are consistent with each other and demonstrate the expected RC-type response to a constant current injection, in the membrane current temporal profile.

Although we have not yet demonstrated that the proposed circuits can produce oscillatory behaviors, such as bursting activation patterns, the positive feedback and the spike frequency adaptation mechanisms implemented make this VLSI model equivalent to the "adaptive exponential integrate-and-fire" (aEIF) model recently proposed in [17]. In [17] the authors demonstrate that aEIF models can accurately predict the spike trains of detailed Hodgkin-Huxley type models, driven by realistic conductance-based synaptic inputs. Therefore we argue that the circuit described in this work can implement faithful models of real neurons, while at the same time satisfying the compactness, low-power, and compatibility with asynchronous logic constraints.

ACKNOWLEDGMENT

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