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Bartolozzi, C; Nikolayeva, O; Indiveri, G

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Abstract

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Chiara Bartolozzi
Italian Institute of Technology
via Morego 30, IT-16163, Genova, Italy
Email: chiara.bartolozzi@iit.it

Olga Nikolayeva
and Giacomo Indiveri
Institute of Neuroinformatics
University - ETH Zurich
Winterthurerstrasse 190, CH-8057 Zurich, Switzerland
Email:giacomo@ini.phys.ethz.ch

***Abstract*— Homeostatic plasticity acts to stabilize firing activity in neural systems, ensuring a homogeneous computational substrate despite the inherent differences among neurons and their continuous change. These types of mechanisms are extremely relevant for any physical implementation of neural systems. They can be used in VLSI pulse-based neural networks to automatically adapt to chronic input changes, device mismatch, as well as slow systematic changes in the circuit's functionality (*e.g.* due to temperature drifts). In this paper we propose analog circuits for implementing homeostatic plasticity mechanisms in VLSI spiking neural networks, compatible with local spike-based learning mechanisms. We show experimental results where a homeostatic control is implemented as a hybrid SoftWare/HardWare (SW/HW) solution, and present analog circuits for a complete on-chip stand-alone solution, validated by circuit simulations.**

I. Introduction

Systems interacting with the real world in an intelligent way need to modify themselves to learn and adapt to the statistics of the input signals, while maintaining their activity within functional ranges, to keep a stable and homogeneous computational substrate. In biological neural systems these opposing requirements are driven by local learning mechanisms that induce changes in the weights of individual synapses of the network, acting on time scales ranging from milliseconds to minutes, and by global stabilizing homeostatic mechanisms that operate on longer time scales (ranging from minutes to hours) and are not synapse-specific [1], [2]. These mechanisms act to stabilize learning processes and ensure a homogeneous computational substrate despite the inherent differences between neurons, the continuous turnover of their constituents and chronic changes of their environment [2].

Despite many implementations of Hebbian learning mechanisms that comprise forms of stabilization [3] and synaptic competition [4], [5] have been proposed, very few attempts have been made to implement explicit global homeostatic plasticity mechanisms, in parallel with classical local learning ones [6]. However, it has been recently argued that the interplay between local Hebbian and global homeostatic processes can have complementary roles [5], or even important synergistic effects [6], allowing for complex behaviors, such as independent component analysis, which would not be possible with either mechanisms alone.

In parallel to the theoretical studies on plasticity in neural networks, a large research effort has been recently devoted to the construction of biologically inspired pulse-based neural systems, particularly via the VLSI neuromorphic approach [7]–[12]. However, the focus has been primarily on the implementation of local short-term spike-based learning algorithms [7], [8], [13], [14], with comparatively little work devoted to global long-term stabilizing processes [15]. In VLSI implementations of neural networks homeostasis could be used to implement a form of automatic gain control to compensate for inhomogeneities due to device mismatch, slow changes in the physical properties of the circuits arising due to temperature drift, or sudden changes in the overall levels of activity in the network (*e.g.* due to activation or inactivation of sub-modules).

Here we propose a set of neuromorphic circuits and methods that implement in parallel both local spike-based plasticity mechanisms and global stabilizing homeostatic mechanisms. The specific form of homeostatic plasticity that we consider in this work is denoted as "activity dependent synaptic scaling" [1]. This multiplicative scaling mechanism acts globally, on the entire population of synapses, and does not affect the relative differences between the synaptic weights, typically induced by local learning mechanisms.

We first demonstrate a mixed SW/HW homeostatic control system that supports both "fast" spike-based learning rules, and "slower" homeostatic synaptic scaling mechanisms (Section II), and subsequently present a novel analog circuit, based on control theory *lag compensation* technique, that implements the homeostatic control algorithm developed and that can be integrated in future neural network chips, for stand-alone VLSI solutions (Section III). To our knowledge, this is the first physical system capable of implementing homeostatic plasticity in parallel with spike-timing dependent plasticity.

II. Homeostatic control in spiking silicon neurons

In most pulse-based neural network chips, neurons have an architecture of the type shown in Fig.1: a series of synapses receive separate spiking input signals and produce output currents that are integrated by the soma circuit. The soma is typically an integrate-and-fire (I&F) neuron that produces an output spike train at a rate proportional to the sum of

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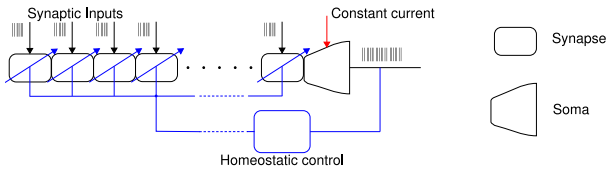

Fig. 1. General homeostatic control scheme for a typical VLSI integrate and fire neuron: synaptic input spikes drive "fast" spike-based learning circuits; post-synaptic spikes are used to modulate global synaptic scaling parameters for stabilizing the neuron's spiking activity. An external constant current can be injected in the soma to modulate its baseline activity.

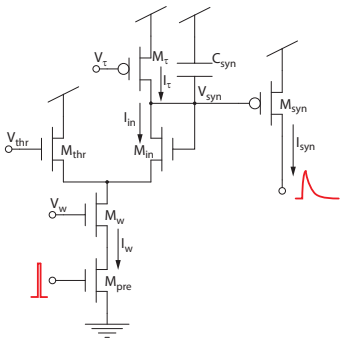

Fig. 2. Diff-Pair Integrator synapse. Input spikes activate the circuit and generate the output current I_{syn} that has an exponential profile over time. The current amplitude is set by V_w and V_{thr}, while its time constant is set by V_τ

all its synaptic currents. While local spike-based plasticity circuits can be used to implement Hebbian-type learning in each synapse block, the homeostatic control block globally adapts the gain of all the synapses afferent to that neuron, to keep its average firing rate close to a target frequency.

A. The Diff-Pair Integrator

A circuit that can implement both global synaptic scaling and local spike-based learning, is the "Diff-Pair Integrator" (DPI) synapse [16], shown in Fig.2. Input spikes activate the M_{pre} transistor and allow current to flow through the differential pair. The M_w transistor weighs the input current depending on the magnitude of the V_w voltage. This voltage can be modified by spike-driven synaptic plasticity circuits, such as the ones proposed in [7], [8], [13], [14], [17], to implement local learning rules. The voltage V_{thr} sets a second independent gain parameter, used for our homeostatic control algorithm, while the voltage V_τ determines the duration of the Excitatory Post-Synaptic Current (EPSC) I_{syn}.

Assuming all transistors operate in the subthreshold regime and are saturated, the DPI's transfer function is [16]:

$$\tau \frac{d}{dt} I_{syn} + I_{syn} = \frac{I_w}{I_\tau} \frac{I_{syn}}{1 + \frac{I_{syn}}{I_g}} \qquad (1)$$

where $\tau = U_T C_{syn}/\kappa I_\tau$, U_T is the thermal voltage, κ the subthreshold slope factor, V_{dd} the power supply voltage, and I_g is a *virtual* current not tied to any MOSFET in the circuit defined as $I_g = I_0 e^{-\frac{\kappa(V_{thr}-V_{dd})}{U_T}}$.

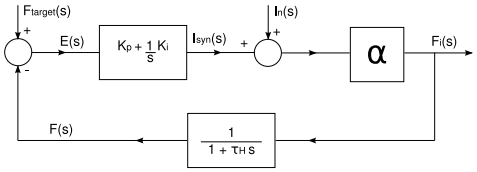

Fig. 3. Mixed HW/SW system control diagram: $F_t(s)$ is the desired target firing rate. The current $I_{syn}(s)$ is produced by the PI-control block. The current $I_n(s)$ represents the "disturbance" signal that is used to model chronic or slow-varying changes in the neuron's net input current. The α block represents the I&F soma that linearly converts its input current into the firing rate $F_i(s)$. The feedback block integrates the neuron's output frequency $F_i(s)$ over time. The resulting low-pass filtered frequency $F(s)$ is then compared to the target frequency $F_t(s)$. The error signal $E(s)$ is used to drive the PI-control block.

For $I_{syn} \gg I_g$, the non-linear eq.(1) reduces to a classical low-pass filter equation:

$$\tau \frac{d}{dt} I_{syn} + I_{syn} = \frac{I_w I_g}{I_\tau} \qquad (2)$$

Under these assumptions, when the synapse receives input spike trains of mean frequency f_{in}, its steady-state mean output current can be described as:

$$\langle I_{syn} \rangle = \left(\frac{I_g I_w}{I_\tau} \right) \tau f_{in}. \qquad (3)$$

B. Homeostatic control in a mixed SW/HW system

In a first stage, to explore different control strategies, we implemented homeostasis as a software algorithm on a workstation interfaced to a VLSI chip comprising a low-power I&F neuron [7] and a DPI synapse [16]. The chip was fabricated using a standard 0.5μm CMOS technology via the MOSIS consortium. The workstation was used to send sequences of spikes to the DPI synapse, and to monitor the output spiking activity of the I&F neuron. To modulate the DPI's I_g gain current we modified the V_{thr} bias voltage via an external voltage source, controlled by the same workstation. The voltage V_w is set by an external voltage reference. To model an average input current produced by the neuron's full dendritic tree, and used to induce a base activity level, we injected a current I_n into the neuron's membrane capacitance. The amplitude of the I_n current was also controlled by the workstation interfaced to the chip. The sequences of spikes sent to the DPI conversely represent the synapse's input signal that could drive local spike-based learning circuits.

We carried out experiments analogous to the ones performed on real neurons,simulating the onset of chronic changes in the system: we fixed the statistics of the input spike trains to the DPI and varied the neuron's input current I_n. The goal of the homeostatic control mechanism is to adapt to these chronic changes on slow time scales, keeping the neuron's average firing rate close to a set target, and without being affected by fast fluctuations in the neuron's net input current. The control strategy adopted in our system is that of a classic PI-controller, as shown in Fig.3: the software algorithm continuously monitors the neuron's firing rate, in real-time, and determines how to scale the synaptic current by measuring

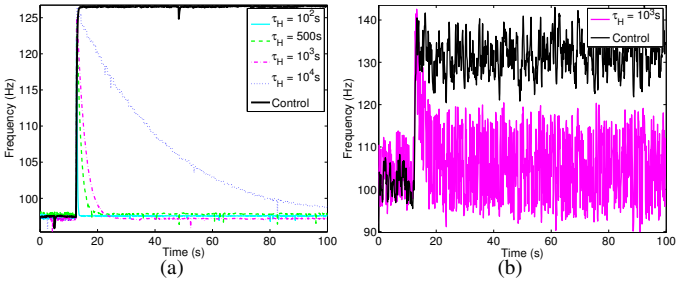

Fig. 4. Homeostasis measurements in the mixed SW/HW system (a) I&F neuron's response to a step DC shift in the VLSI neuron's input current. The thick black line shows the output of the neuron for the case in which homeostatic control is not enabled. The other curves show the effect of the control algorithm as a function of the parameter τ_H. (b) Neuron response to DC shifts in the input current superimposed to high frequency fluctuations: the DC offset in the firing rate is adapted out, while the high frequency component of the input signal passes through.

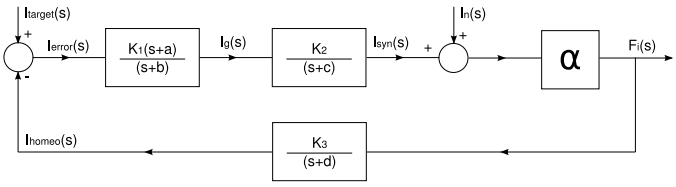

Fig. 5. Lag compensator control diagram.

the error between the neuron's firing rate and a target firing rate, and by computing its integral over time. The change in synaptic scaling is then induced by modulating the V_{thr} bias that acts on I_g.

In Fig.4(b) we show measurements from the HW/SW system for the control case: we combined current injection and synaptic stimulation such that the neuron fired at a desired rate of approximately 98Hz and then produced chronic change in the I&F neuron's firing rate by applying a step increase in the current I_n. As expected, the PI control algorithm adapted the neuron's firing rate back to its target value with different time constants depending on the values of τ_H.

To show that the "slow" homeostatic mechanism does not interfere with "fast" spike-based learning mechanisms we superimposed high-frequency fluctuations to I_n and repeated the experiment. As shown in Fig.4(b), the DC offset is removed while the high frequency fluctuations are transmitted by the I&F neuron. The amplification of the high-frequency components is due to the choice of the K_i, and K_p parameters in the control algorithm.

III. Analog VLSI implementation of the homeostatic control algorithm

We designed a set of analog circuits to implement the software control algorithm on-chip. Due to the non-idealities of VLSI integrator circuits, we used *lag compensation* control, shown in Fig.5, instead of pure PI control scheme of Fig.3.

We implemented such scheme with a full-custom analog design using compact low-power (subthreshold) circuits shown in Fig.6. The relationships between the parameters of Fig.5 and

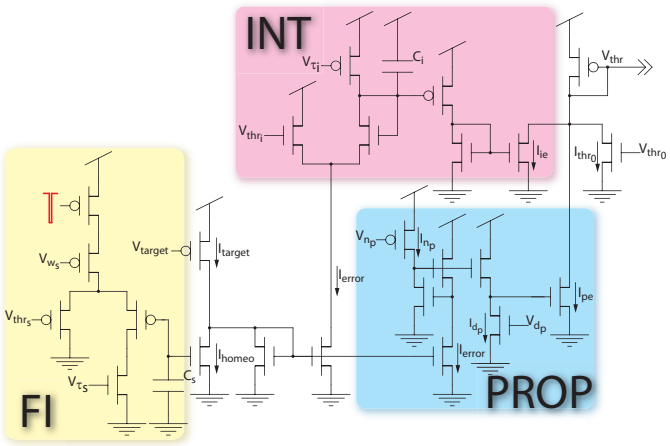

Fig. 6. Lag compensation circuit: the FI block integrates the I&F neuron's spiking output, while the PROP and the INT blocks calculate the proportional and integrated components of the control signal, respectively. The sum of the I_{thr_0}, I_{pe} and I_{ie} currents determines the value of the V_{thr} bias, which globally affects all synapses afferent to the neuron as shown in Fig.1.

the circuit variables are defined as follows:

$$K_1 = \frac{I_{n_p}}{I_{d_p}} \qquad K_2 = \frac{I_w \kappa}{C_{syn} U_T} \qquad K_3 = \frac{I_{w_s} I_{g_s} \kappa}{C_s U_T}$$

$$a = \frac{1}{\tau_i} + \frac{I_{g_i} \kappa I_{d_p}}{C_i U_T I_{n_p}} \qquad b = \frac{1}{\tau_i} \qquad c = \frac{1}{\tau} \qquad d = \frac{1}{\tau_s},$$

where the τ variables are defined as:

$$\tau_i = \frac{U_T C_i}{\kappa I_{\tau_i}} \qquad \tau_s = \frac{U_T C_s}{\kappa I_{\tau_s}} \qquad \tau = \frac{U_T C_{syn}}{\kappa I_\tau}$$

The frequency integration (FI) block consists of a DPI circuit that integrates the output spikes of the I&F neuron into the I_{homeo} current. The I_{error} current is generated by comparing the FI block output to the target current I_{target} , set by the constant external bias voltage V_{target} . The integration (INT) block uses another instance of the DPI circuit to integrate the error current over time, producing the I_{ie} current. The proportional (PROP) block uses a translinear multiplier [18] to multiply the I_{error} current by constant scaling factors set by V_{n_p} and V_{d_p}, producing the I_{pe} current.

The control circuit acts on the V_{thr} bias voltage, which can be connected globally to all DPI synapses afferent to the neuron, to scale their outputs via the I_g current. The proper value of V_{thr} is computed on the top right part of the circuit of Fig.6, by summing the I_{thr_0}, I_{pe} and I_{ie} currents.

A. Circuit simulation results

We used TSPICE for circuit simulations. To speed up circuit simulation times, we did not simulate the I&F neuron: assuming that the neuron's firing is linearly proportional to its input currents, we sourced the sum of I_{syn} and I_n in the V_s node of Fig.6. As for the mixed SW/HW experiments, we fixed I_{syn} and varied I_n to model chronic changes and trigger the homeostatic control.

Fig.7(a) shows the transient simulation results for a step decrease in I_n: to compensate for lower net input currents, the

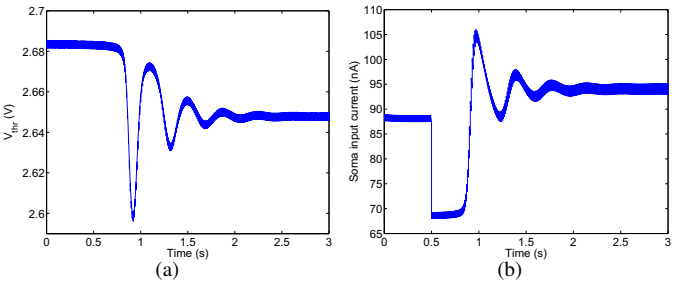

Fig. 7. System response to I_n step decrease at t=0.5s. (a) After few oscillations, V_{thr} decreases in order to increase I_{syn}, thereby compensating for I&F input current change. (b) After the step decrease, the total input current to the I&F neuron is restored by the homeostatic control to a value lying within the control mechanism's tolerance range.

synapse increases its gain via I_g; as I_g depends exponentially on $(-V_{thr})$, the circuit decreases its value accordingly.

Fig.7(b) shows how the neuron's net mean input current adapts to the chronic change: the control circuit scales I_{syn} to counteract the effect of the step change in I_n.

IV. Conclusions

Homeostasis is one of the strategies used by biological systems to cope with inhomogeneities and continuous changes of their components while maintaining the capability of learning and adapting to new stimuli. Multiplicative synaptic scaling is a specific type of homeostatic adaptation that has been observed in cultures of cortical, spinal and hippocampal neurons [1], as well as *in vivo* [19]. In this paper we proposed a possible circuit implementation of the homeostatic synaptic scaling obtained by combining the HW transposition of a lag compensated control algorithm, with a neuromorphic synaptic circuit that supports both Hebbian type of spike-driven plasticity mechanisms as well as global synaptic scaling.

The specific role of homeostatic plasticity mechanisms, with respect to other forms of Hebbian learning is actively being investigated. The system proposed here, and validated for a single neuron-single synapse system, can be implemented on chips comprising large arrays of silicon neurons and synapses and used as a tool to test different computational theories, in real-time, with real-world stimuli.

In such a system all of the synapses converging to a single neuron will be globally scaled by the proposed circuitry to implement synaptic homeostasis and maintain the activity of each neuron within a functional range, thus counteracting the effect of device mismatch. In addition the new analog homeostatic control circuit designed can be used as a form of global automatic gain control to adapt the system to chronic changes in the input configuration as well as to counteract slow changes in the circuit's response properties. This mechanism is compatible with conventional engineering solutions for minimizing the effects of mismatch, or compensating temperature drifts, and can be especially useful to compensate for the increasing number of defects expected in the future scaled CMOS processes.

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