BIAS CURRENT GENERATORS WITH WIDE DYNAMIC RANGE

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ABSTRACT

This paper describes CMOS circuits that generate a wide-ranging set of fixed bias currents, spanning at least 6 decades down to picoamperes. A master current generated by a bootstrapped current reference is successively divided by a current splitter to generate the desired references. An unpublished startup circuit and a novel power control mechanism are described. Measurements from a 0.35u implementation are presented and non-idealities are investigated. Readers are directed to a design kit that makes it simple to generate the layout for a bias generator with a set of desired currents for scalable MOSIS CMOS processes.

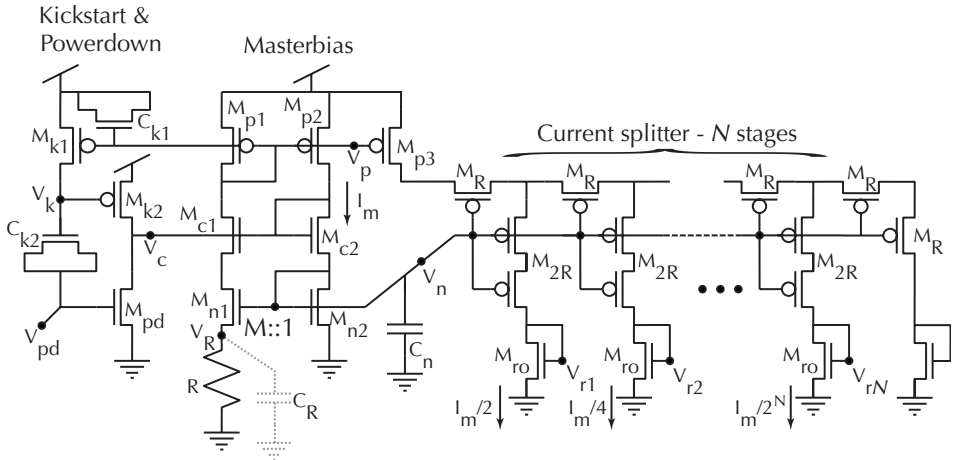
1. INTRODUCTION

Analog or mixed-signal CMOS chips usually require a number of fixed reference currents for biasing amplifiers, determining time constants and pulse widths, powering loads for static logic, etc. The required currents can span a wide range, for instance if the dynamics of the circuits span timescales from nanoseconds to seconds. (For example, a g_m-C filter with a time constant of 10ms and C=1pF requires a bias current of about 1pA.) Often in experimental chips these references are left out because designers assume that these "standard" circuits could be easily added when the design is productized. As a result, chips are designed that must be individually tuned for correct operation by setting gate voltages that depend on chip-to-chip variation in threshold voltage, and any secondary user must be tutored on the tuning of the parameters. This style of design does not allow one to assess if the chip could actually be manufactured in quantity. Another motivation for including a bias generator circuit on chip is that other manufacturable means for generating very small currents are problematic given that they imply huge resistance values, or threshold-dependent gate voltages.

Here we show the architecture of bias generator circuits that derive a wide-ranging set of fixed bias currents from a single master current. We describe the master bias, the startup and power control circuits, the use of current splitters to derive smaller currents, discuss measurements from fabricated circuits, and describe a bias generator design kit that automates the production of bias generator layout. We have built this style of bias generator in 1.6u, 0.8u, and 0.35u processes, but here we only show the latest results from the 0.35u implementation, which came from the layout generated by the design kit.

2. BIASING CIRCUITS

The circuit shown in Figure 1 generates the bias currents. All the individual bias currents are scaled copies of the single master current I_m. The master current is subdivided to form a set of smaller references and these references are copied by the circuits in Figure 2 to form the individual biases.



Transistor W/L	
M_{n2}	24/6
M_{n1}	M*24/6
M_{p1}, M_{p2}, M_{p3}	76/65
M_{c1}, M_{c2}	24/6
C_{k1},C_{k2}	132/20
M	40
M_R, M_{2R}	24/12
M_{pd}, M_{k1}, M_{k2}	6/6
Capacitance	
C_n	~10pF
C_{k1},C_{k2}	~1pF

Figure 1 Bias generator circuits. Transistor sizes are in units of λ (scalable parameter) All sizes are 24/6 unless listed above. C_{k1} & C_{k2} are MOS capacitors. M_{2R} are unit transistors.

2.1 The master bias

The master current I_m is generated by the familiar bootstrapped current reference attributed to Widler and first reported in CMOS by Vittoz et al. in [1] (see also [2;3], for example). Transistors M_{n1} and M_{n2} have a gain ratio $(W_{n1}/L_{n1})/(W_{n2}/L_{n2})=M$. Since the currents in the two branches are forced to be the same by the mirror M_{p1}-M_{p2}, the ratio in current density in the M_n's sets up a difference in their gate-source voltage, which is expressed across the load R. Resistance R and ratio M determine the current. The master current I_m that flows in the loop is computed by equating the currents in the two branches. In subthreshold, this yields $I_m = e^{kV_n/U_T} = Me^{(kV_n - I_m R)/U_T}$, resulting in the remarkably simple yet accurate formula

$$I_m = \ln(M)\frac{U_T}{R}, \quad U_T = \frac{kT}{q} \qquad (1)$$

Above threshold, an analogous computation yields another formula which is not very accurate but still useful:

$$I_m = \frac{2}{\beta R^2}\left(1 - \frac{1}{\sqrt{M}}\right)^2, \quad \beta = \mu C_{ox}\frac{W_{n2}}{L_{n2}} \qquad (2)$$

The data in Figure 3 shows that the estimated I_m is the maximum of (1) and (2). With ideal transistors, I_m does not depend on supply voltage or threshold voltage, but is monotonic in temperature (approximately PTAT in subthreshold). In reality it is slightly affected by the supply voltage through drain conductance, and also by mismatch of the threshold voltage and β between the transistors in the current mirrors.

To increase the power supply rejection ratio, the drain resistances of the transistors are increased by using long $M_{p's}$ and cascoding M_{n1} with M_{c1} and M_{c2}. This choice minimizes the size of the entire generator.

The ratio M is not critical as long as it is substantially larger than 1. We have used values from 20 to 120, and the measurements shown here used M=40. A very large ratio can destabilize the circuit through the parasitic capacitance C_R on V_R. A common error in this circuit is to have too much capacitance to ground at V_R; this excessive capacitance causes large-signal limit-cycle oscillations. The circuit can be stabilized by making the compensation capacitor C_n several times C_R. In practice, we usually bring out V_n to ensure that the master bias can be stabilized.

2.1.1 Startup and power control

A startup circuit is necessary to avoid the stable zero-current operating point. Transistors M_{k1}, M_{k2}, M_{pd}, and MOS capacitors C_{k1} and C_{k2} enable the startup and power control functionality. The loop is kick-started when powered up by the current flowing from M_{k2}, which is on until V_k is charged to Vdd by M_{k1}, which then shuts off. C_{k2} holds V_k low on power-up (V_{pd} is at ground), while C_{k1} ensures that V_p is initially held near Vdd, holding M_{k1} off so that the kickstart can occur. C_{k1} and C_{k2} must be large enough that sufficient charge flows into the loop to get it going; we usually use about 1pF. C_{k1} and C_{k2} are MOS-capacitors to avoid the necessity of a special capacitor layer like Poly2. Their polarity is arranged so that they operate in inversion when they need to. While the bias generator is operating, essentially zero current flows in the startup circuit. The inventors of this startup circuit desire anonymity.

V_{pd} allows for soft power control by a novel mechanism. V_{pd} is tied to ground for normal operation. Raising V_{pd} to Vdd turns off the master bias and the derived biases, by pulling V_c to ground and shutting off the current in the loop. Yanking V_{pd} to ground yanks V_k low, through C_{k2} (M_{k1} is off), and the kickstart restarts the current as before. While V_{pd} is high, no current flows in M_{pd} because V_k is at Vdd and M_{k2} is off. A stray DC path to ground from V_n (say, across C_n) could require pumping V_{pd} for a few cycles, but if there is no DC path other than through M_{n2}, a single downward transition on V_{pd} is sufficient for restart (Figure 4).

2.2 The current splitter

The master current is copied to a Bult and Geelen [4] current splitter and divided successively by it to form a geometrically-spaced series of smaller currents. At each branch, a fixed fraction of the current is split off, while the rest continues to later stages. The last stage is sized to terminate the line as though it were infinitely long. The current splitter principle accurately splits currents over all operating ranges from weak to strong inversion, independent of everything but the effective device geometry. Figure 1 shows an R-2R splitter—built from unit transistors—that splits by octaves, but we have also built decade splitters by using M_R and M_{2R} with different aspect ratios. However, we strongly recommend the use of unit transistors. We have discovered subtle effects of body bias and operating range that act differentially on transistors with differing aspect ratios. These effects cause non-ideal splitter behavior, especially in deep subthreshold.

M_R and the two M_{2R} transistors form the R-2R network; the octave splitter is terminated with a single M_R transistor. The splitter has N stages; the current at the k^{th} stage is $I_m/2^k$. The final current is the same as the penultimate current. Our transistor sizing for the octave splitter is given in the table in Figure 1. The reference voltage for the p-FET gates in the splitter is the master bias voltage V_n.

The diode-connected M_{ro} transistors read out the currents to make copies for individual biases. This arrangement allows for non-destructive readout at the cost of mismatch in the M_{ro} transistors.

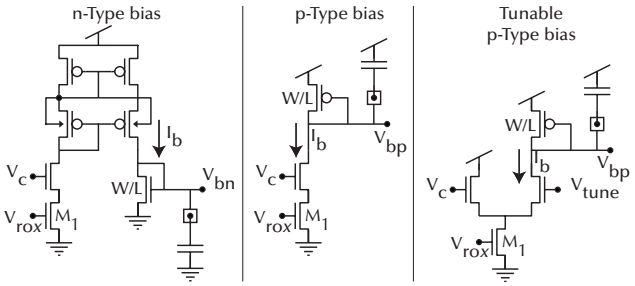


Figure 2 Generating individual biases from the current splitter outputs. M_1 has same W/L as M_{ro} in Figure 1.

An individual bias (V_{bn}, V_{bp}) is generated by copying a splitter current using one of the cells shown in Figure 2 (using a cascode for more accuracy) into a diode-connected transistor with the desired W/L ratio. The resulting gate voltage is then used as the bias voltage. The p-type mirror used for the n-type bias is also cascoded for more accuracy and the bulks of the cascode transistors are tied to their source. (This arrangement provides a bit more headroom because the back-gate bias is reduced, which reduces the required gate-source voltage.) The last arrangement, using a differential pair, enables fine tuning of the programmed bias in a controlled manner by external input V_{tune}. Tying V_{tune} to V_c programs half the splitter current, and the actual value can be varied from 0 to the full splitter current.

A diode-connected transistor operating in subthreshold has conductance $g = \kappa I_b / U_T$. That means the bias voltage for a small bias current has high impedance and can easily be disturbed by capacitive-coupled transients on other signals. The simplest solution is to bypass the bias with a large capacitance to the appropriate power rail (Figure 2), which is easy to do if the bias is brought off chip. In a production chip, the pad may not be economically justifiable, but in a prototype chip we strongly advise to bring all biases out to pads anyway.

3. MEASURED CHARACTERISTICS

We have used these bias generators in several generations of CMOS process technology (1.6u, 0.8u, and 0.35u) with no striking differences in performance. Here we show some measurements and discuss the limits to operation. All the results shown here come from a bias generator with a 20-stage octave splitter built in a 0.35u process. The layout for this bias generator was generated by the design kit discussed in Section 4.

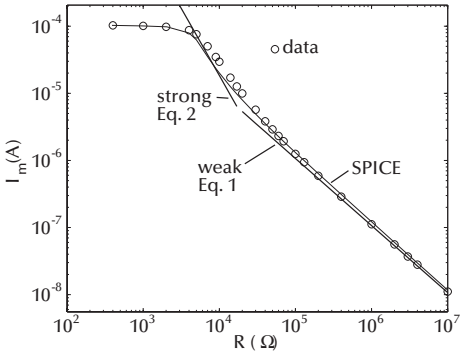


Figure 3 Master current I_m vs. resistance R

The variation in master current with resistance R is shown in Figure 3, along with the theoretical values given by Equations (1) and (2), and SPICE simulation results. The theory gives a reasonable estimate for the measured values, and the SPICE simulation does even better. The exact behavior is not really important for practical purposes because R is generally external and is selected for the desired operating point. The maximum current is determined by the power supply rails and the headroom required by the current mirrors.

The power control behavior is shown in Figure 4. V_{pd} is initially high (the powered off state) and is then brought low. V_n goes from near zero to the stable value, following an exponential. C_n=10nF was used to demonstrate that a large C_n does not affect restart except to delay it.

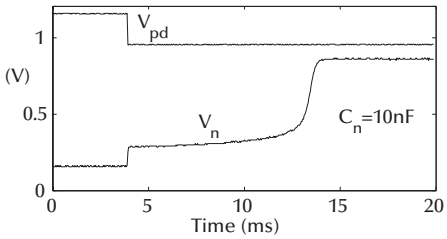


Figure 4 Power control with V_{pd}. (V_{pd} is rescaled). There was a 30 second delay since the last cycle.

The behavior of the octave splitter is shown in Figure 5. It is amazingly ideal over 20 octaves (6 decades) spanning strong to weak inversion. A current of 10pA is reliably generated from a master current of 10uA.

Imagers or focal plane arrays require biases that are not affected by illumination. In the design kit layout, the splitter and individual bias devices are protected from parasitic photocurrents by being covered with metal and surrounded by n-well guard bars. Immunity to illumination is demonstrated in the data shown in Figure 6. Direct illumination with 500 lux slightly increases I_m, but has essentially no direct effect on the splitter currents, even at the smallest currents. That means that this layout is suitable for use in imagers or focal plane arrays.

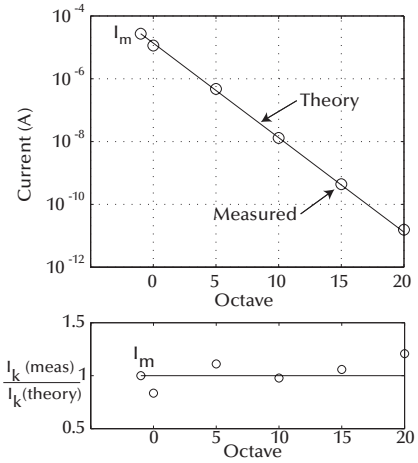


Figure 5 Octave splitter behavior.

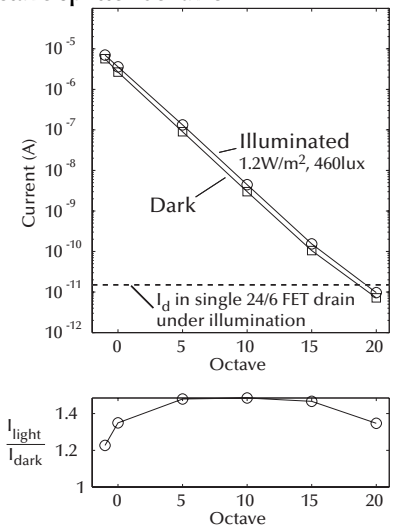


Figure 6 Effect of illumination on generated currents.

The smallest current that can be generated is limited not by the splitter, but rather by the off current of transistors. In the case of the measured chip, this I_0 is about 1pA. The minimum possible generated current is a few times I_0. The currents in the last stages of the splitter can approach the junction leakage currents, but a bias generated from these currents is limited to the off current, because the bias transistors are presumably in saturation. Generation of still smaller currents would need to employ techniques such as those outlined by [5], where the splitter output current is directly used as the bias and the current is copied with a source-biased current mirror.

4. DESIGN KIT

One of the authors (Delbrück) has developed a design kit that makes it simple to construct a complete bias generator when using Tanner (www.tanner.com/eda) design tools. The desired bias currents are specified in the schematic, using parameter cells. A compiler parses the netlist from the schematic, computes the range of biases, the number of required splitter cells, and the master bias current. It then builds the layout of the complete generator using a set of predefined cells combined with generated routing. Readers are referred to www.ini.unizh.ch/~tobi/biasgen. The cells are constructed to be used with MOSIS (www.mosis.org) scalable λ-based design rules, with 2 metal, single poly processes, so the layout is compatible with any MOSIS CMOS process down to 0.35u. (Finer processes require slight modification to contact sizes and metal spacing.) The cells are shielded by metal and have guard rings, so they are suitable for use in imager or focal plane arrays. A compiled bias generator in 0.35u was the source of most of the data presented here.

5. CONCLUSION

Chips with known requirements for a wide range of bias currents can benefit significantly from the use of the circuits described here. The authors have supplied and sold chips equipped with these circuits to naïve users. Use of chips by naïve users can be made much easier to support if the parameters are truly fixed and not dependent on fine tuning of external parameters, and the chip designers can feel a satisfaction that they understand the operation of the chip and that it could probably be manufactured in quantity. The design kit described here makes it simple to add these biasing circuits to any MOSIS chip and to be reasonably confident that they will function correctly the first time.

6. ACKNOWLEDGEMENTS

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