FLOATING GATE ANALOG MEMORY FOR PARAMETER AND VARIABLE STORAGE IN A LEARNING SILICON NEURON

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Abstract

Retention of parameters and learnt synaptic weights is a central problem in the construction of neural networks. We have applied analog floating gate technology to solve these problems in the context of biologically realistic 'silicon neurons'. Parameters are stored on a novel floating gate array, and synaptic weights are retained by a floating gate learning synapse, that performs on-chip learning. The latter can emulate a form of long term potentiation (LTP) and long term depression (LTD) as observed in biological neurons.

1 Introduction

CMOS aVLSI technology is being used to implement bio-inspired neuronal circuits [5, 7]. However there are limits on how closely researchers can approximate relevant neuronal properties. Two such limits are addressed and solved in this paper: the limit in numbers of analog parameter voltages, and the problem of retaining the values of variables of adaptation and learning.

The need for many analog parameter voltages has limited the sophistication of analog chips in general, and of neuromorphic hardware in particular. Unlike digital circuits, analog ones require analog biases. The number of chip pins used to limit the number of these parameters. An alternative is to store the analog parameters on-chip, using volatile capacitive storage, and access them via a few address lines. This method requires refreshing, e.g. via an external digital memory and a digital-analog converter (DAC). This approach has the disadvantage that the refresh and the switching of the digital control line induce noise in the analog values. Static digital on-chip storage of these parameter voltages reduces these problems but with a desired resolution of 10 bits, the basic circuit requires 20 transistors for an ADC and a further 60 transistors for 10 storage flip flops and so occupies too large an area.

We used the floating gate (FG) memory cell proposed by Diorio and colleagues [2] to construct a FG analog random access memory (aRAM). A similar memory with sequential access has been introduced by Harrison et al. [4]. FGs are isolated conductances that can be charged by Fowler-Nordheim Tunneling and discharged using hot electron injection. Since the charge cannot escape through the insula-

tion, it is retained thereafter. A FG-aRAM needs few pins, no refresh and not so much space. Most importantly the memory's content is retained even when the power supply is off. A disadvantage is the necessity of a high voltage bias (about 33V) the handling of which requires some precautions. That voltage can be reduced by using non-standard and more expensive CMOS production processes.

Even more demanding is the permanent storage of analog *variables* that are changed according to an on-chip adaptation circuit (e.g. weight storage in on-chip learning). We use FG memory cells in our silicon neuron for analog synaptic weight storage; using a particular learning synapse we can emulate a form of biological long term potentiation (LTP) and long term depression (LTD).

2 The silicon neuron

The silicon neuron in this work consists of a single compartment soma with a leakage conductance, sodium and potassium spike conductances, a high-threshold calcium conductance and a calcium-dependent potassium conductance [7, 5]. Almost all parameters (28) are set by cells in the FG-aRAM (with the exception of four that draw more current than our cells could provide) and represent analog values for setting the time and voltage dependence of the ionic conductances.

Additionally, the soma has four learning synaptic conductances. They are simple excitatory synaptic conductances and we will call them AMPA synapses [7]. One of the AMPA synapses' parameters sets the amplitude of its EPSP. We will call that parameter the synaptic weight. The learning mechanism described in section 4 controls these four parameters which are stored on four FG memory cells.

3 Storing parameters for a silicon neuron

Our memory permits the retention of analog voltages for years. This storage is achieved using floating gates: totally isolated capacitances. By means of tunneling and hot electron injection one is able to change their potentials which otherwise remain constant. This technique has been used for many years in a digital manner in electrically erasable programmable read-only memories (EEPROMs), but only lately for analog purposes. The basis of a single memory cell consists of such a floating gate and a high gain amplifier and has been proposed by Diorio [2]. We added addressing logic and a read line to an array of single cells to make an aRAM. Due to the presence of a high voltage switch per cell, their voltages can be moved up and down individually. Four biases are needed to operate the memory, two of them above 5V ($\sim$33V,$\sim$20V). A total of 12 chip pins are needed for 32 parameters (4 parameters, read out, up and down, 5 address bits). The actual layout area of the whole block is 343 x 1865 μm^2 in the $2\mu m$ bi-CMOS process used. Full layout can be obtained via the first authors homepage (http://www.ini.unizh.ch/~hafliger).

Changing a cell's value is very slow, in the order of 100mV per second. However, in our application, speed is not important. The memory cells are used like the potentiometers they replace: voltages are adjusted up and down by hand with switches or automatically via a computer with digital I/O lines for switching and addressing and an ADC for comparison to a target voltage (we use a NI LabPC card).

Standard deviations of the floating gate memory cells' contents during a 12 hour recording and after one week during which the chip was turned off, were in the same order of

accuracy as in our measuring setup (∼3mV). This corresponds to a resolution of at least 10 bits. That accuracy proved to be perfectly sufficient for our requirements. The neuron operated stably during 2 days of testing and again after a one week interval.

4 Regulation of synaptic efficacy

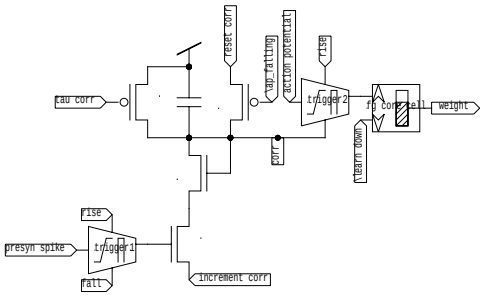

Figure 1: Schematics of our learning mechanism in the AMPA synapse [7]. Digital pulses from simple positive edge triggered monostables [3] (pulse widths controlled by $fall$ for trigger 1 and *corr* for trigger 2) make the synaptic weight (controlling the EPSP amplitude) in a FG memory cell increase or decrease. *tau corr*, *reset corr*, *increment corr*, $rise$ and $fall$ are fixed parameter voltages. $\backslash learn\ down$ and $\backslash ap\ falling$ are active low pulses triggerd by the *action potential*, the first by the rising, the other by the falling edge.

The learning synapse is a descendent of our earlier version with volatile weight storage, that we modelled to approach the 'modified Riccati rule' (MRR) [3]. It is a local learning rule, sensitive to temporal correlations of the spike inputs and the output of the cell implemented by 24 transistors, one capacitance and a core memory cell (as used in the aRAM) per synapse. The change in synaptic weight modulates the EPSP amplitude of the four AMPA synapses. So we approximate the behavior observed in [6, 1] (figure 2).

5 Conclusion

Limits in the number of parameter voltages on aVLSI chips are no longer given by the number of pins. Floating gate on-chip analog memory can overcome that restriction in a space-efficient way, which is especially convenient in analog hardware emulating biological processes in detail. Also non-volatile dynamic variables can be colocalized with the adaptation circuitry, which makes for space- and energy-efficient designs. Furthermore the chip's state (e.g. in learning) is preserved even if the chip is switched off. Learning or other adaptation processes that permanently change an aVLSI circuit's behavior can be implemented using this technique. For example, learning silicon AMPA synapses can emulate a form of LTP and LTD resulting in permanent changes in synaptic efficacy as demonstrated in this paper.

Acknowledgments

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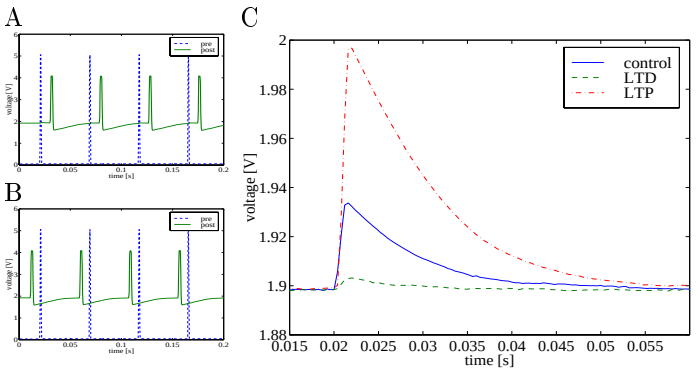

Figure 2: Stimulation patterns used on our AMPA synapse and their effect on subsequent excitatory post synaptic potentials (EPSPs). A and B show two stimulation patterns that lead to LTP and LTD respectively. The presynaptic spikes (dashed lines) are digital pulses delivered to one of the learning synapses, whereas the silicon neuron's output (solid lines) resembles closely biological action potentials (AP). The postsynaptic APs have been forced by stimulating a non-learning synapse that produced single EPSPs that were large enough in amplitude to make the silicon neuron fire. We ensured that the learning synapses EPSP remained below the soma's firing threshold, even when it was increasing. Similarly to [6] we stimulated pre- and post-synaptically with bursts of four spikes with 50ms spacing. We applied 15 such bursts with 200ms inter-burst intervals. The pre- and postsynaptic spikes were shifted by 10ms against each other. When the presynaptic spike preceded the postsynaptic spike (A) the subsequent EPSPs were higher in amplitude (C, dot-dashed line) and if the presynaptic spike followed the postsynaptic one (B), the synaptic efficacy decreased (C, dashed line). Before the experiments the synaptic weight was always brought to the same baseline (C, solid line).

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